Silicon PNP Power Transistors BDV64/64A/64B/64C

DESCRIPTION

·With TO-3PN package
·Complement to type BDV65/65A/65B/65C
·DARLINGTON
·High DC current gain

APPLICATIONS

·For use in general purpose amplifier applications.

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

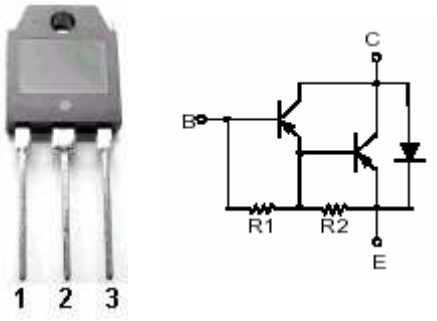

Fig.1 simplified outline (TO-3PN) and symbol

Absolute maximum ratings(Tc=25□)

SYMBOL	PARAMETER		CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	BDV64	Open emitter	-60	V
		BDV64A		-80	
		BDV64B		-100	
		BDV64C		-120	
V_{CEO}	Collector-emitter voltage	BDV64	Open base	-60	V
		BDV64A		-80	
		BDV64B		-100	
		BDV64C		-120	
V_{EBO}	Emitter-base voltage		Open collector	-5	V
I_C	Collector current			-12	A
I_{CM}	Collector current-peak			-15	A
I_B	Base current			-0.5	A
P_C	Collector power dissipation		T_C=25□	125	W
			T_a=25□	3.5	
T_j	Junction temperature			150	□
T_{stg}	Storage temperature			-65~150	□

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	BDV64	I_C=-30mA, I_B=0	-60			V
		BDV64A		-80			
		BDV64B		-100			
		BDV64C		-120			
V_{CEsat}	Collector-emitter saturation voltage		I_C=-5A ,I_B=-20mA			-2.0	V
V_{BE}	Base-emitter on voltage		I_C=-5A ; V_{CE}=-4V			-2.5	V
I_{CBO}	Collector cut-off current	BDV64	V_{CB}=-60V, I_E=0 V_{CB}=-30V, I_E=0;T_C=150□			-0.4 -2.0	mA
		BDV64A	V_{CB}=-80V, I_E=0 V_{CB}=-40V, I_E=0;T_C=150□			-0.4 -2.0	
		BDV64B	V_{CB}=-100V, I_E=0 V_{CB}=-50V, I_E=0;T_C=150□			-0.4 -2.0	
		BDV64C	V_{CB}=-120V, I_E=0 V_{CB}=-60V, I_E=0;T_C=150□			-0.4 -2.0	
I_{CEO}	Collector cut-off current	BDV64	V_{CE}=-30V, I_B=0			-2	mA
		BDV64A	V_{CE}=-40V, I_B=0				
		BDV64B	V_{CE}=-50V, I_B=0				
		BDV64C	V_{CE}=-60V, I_B=0				
I_{EBO}	Emitter cut-off current		V_{EB}=-5V; I_C=0			-5	mA
h_{FE}	DC current gain		I_C=-5A ; V_{CE}=-4V	1000			
V_{EC}	Diode forward voltage		I_E=-10A			-3.5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
$R_{th\ j\text{-}c}$	Thermal resistance junction to case	1.0	□/W

PACKAGE OUTLINE

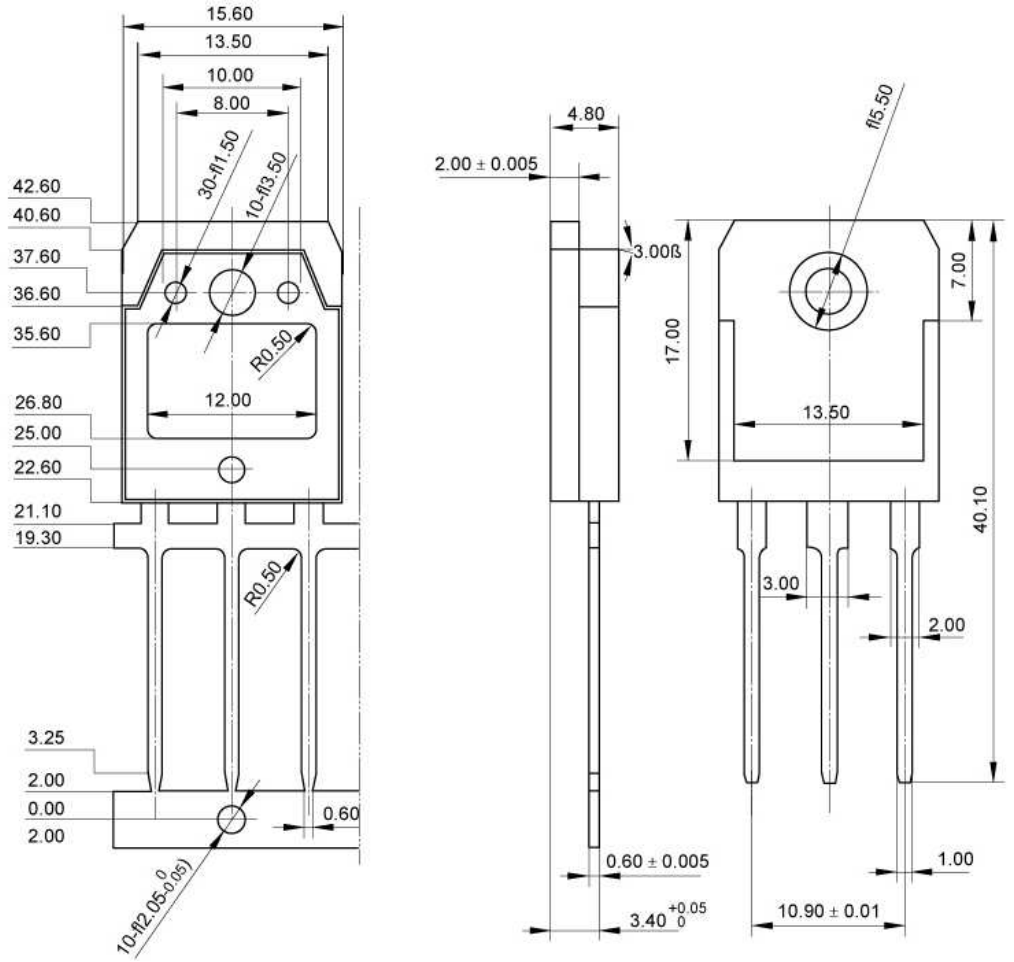

Fig.2 Outline dimensions(unindicated tolerance:±0.1mm)