National Semiconductor

DM75L52/DM85L52, DM75L54/DM85L54 TRI-STATE® Synchronous Counters/Latches

General Description

These circuits logically combine the functions of counters for frequency division, latches to store the data from the counters, and output buffer gates which provide both standard TTL outputs as well as high-impedance outputs for multiplexing of data. The counters are fully synchronous, and are made up of four edge-triggered JK flip-flops. To further facilitate operation, the Count Mode and Terminal Count outputs are also operable when the data outputs are in the high-impedance state or the latch mode.

Features

- DM75L52/85L52 Decade counter/latch
- DM75L54/85L54 Binary counter/latch
- Typical power dissipation 38 mW
- Typical clock frequency 11 MHz

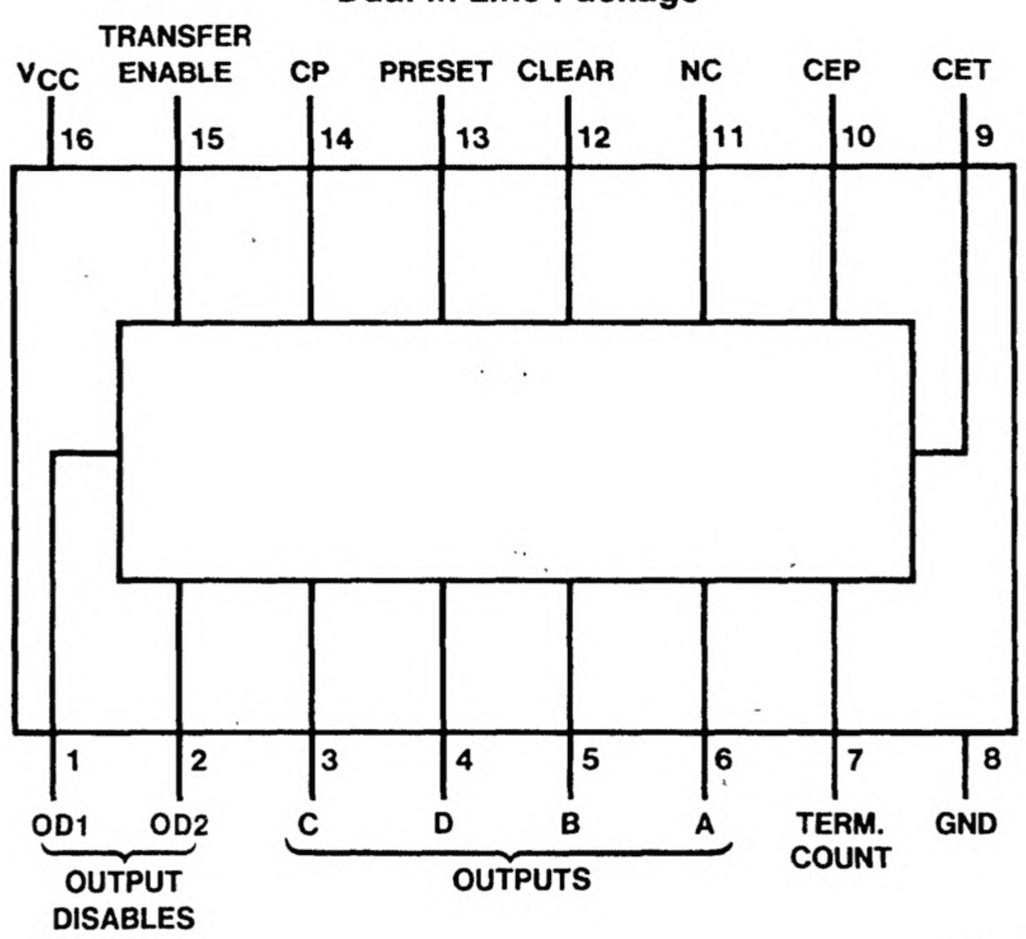
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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75L52 (J) 85L52 (N)
75L54 (J) 85L54 (N)

Function Table

Inputs							Outputs				
OD1	OD2	CEP	CET	Clear	Preset	TE	A	B	C	D	TC
H	X	X	X	X	X	X	"High Impedance State"				*
X	H	X	X	X	X	X	"High Impedance State"				*
L	L	X	X	H	X	H	L	L	L	L	L
L	L	X	X	L	H	H	H	H	H	H	*
L	L	X	X	X	X	L	LATCH				*
L	L	H	H	L	L	H	COUNT				*

*Function of the count sequence.

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
TE = Transfer Enable
TC = Term. Count

Recommended Operating Conditions

Sym	Parameter	DM75L52, L54			DM85L52, L54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current (Except Terminal Count Input)			−1			−1	mA
I_{OH}	High Level Output Current (Terminal Count)			0.2			0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency	0		6	0		6	MHz
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'L52 and 'L54 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM75	2.4			V
			DM85	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM75		0.15	0.3	V
			DM85		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V	CET			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	CET			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	CET			−0.36	mA
			Others			−0.18	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.3V, V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−3		−15	mA
			DM85	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max			7.6	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'L52 and 'L54 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$						Units
		$C_L = 5\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency				6	11			MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					115	220	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					75	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Transfer Enable to Output					90	160	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Transfer Enable to Output					90	160	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					75	150	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					90	150	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		8	15				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		57	105				ns

Mode of Operation

When the Transfer Enable (TE) is at a logical "1" level, the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear resets the counter to 0000.

Asynchronous Preset sets the counter to 1111. The 1111 state may be used in the L52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the L52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the L54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

(L52) $TC = CET \bullet A \bullet \overline{B} \bullet \overline{C} \bullet D$
(L54) $TC = CET \bullet A \bullet B \bullet C \bullet D$

The following logic levels control the device:

- The counters change state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state," either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique.

Counter stages can be cascaded to provide multiple stage BCD or Binary synchronous counting by using the L52 or the L54, respectively. With a Terminal Count (TC) fan out of ten, eleven stages are able to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the TE input while the counters can continue counting. The display can be updated at any time by applying a positive pulse to the TE input.

DM75L52/DM85L52
DECADE COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H
**If Preset Applied					
Next Count	H	H	H	H	L
	H	L	L	L	L

**The 111 state may be used in conjunction with certain decoder/drivers (DM7446A, 7447A, 7448) for blanking leading zeroes.

DM75L54/DM85L54
BINARY COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

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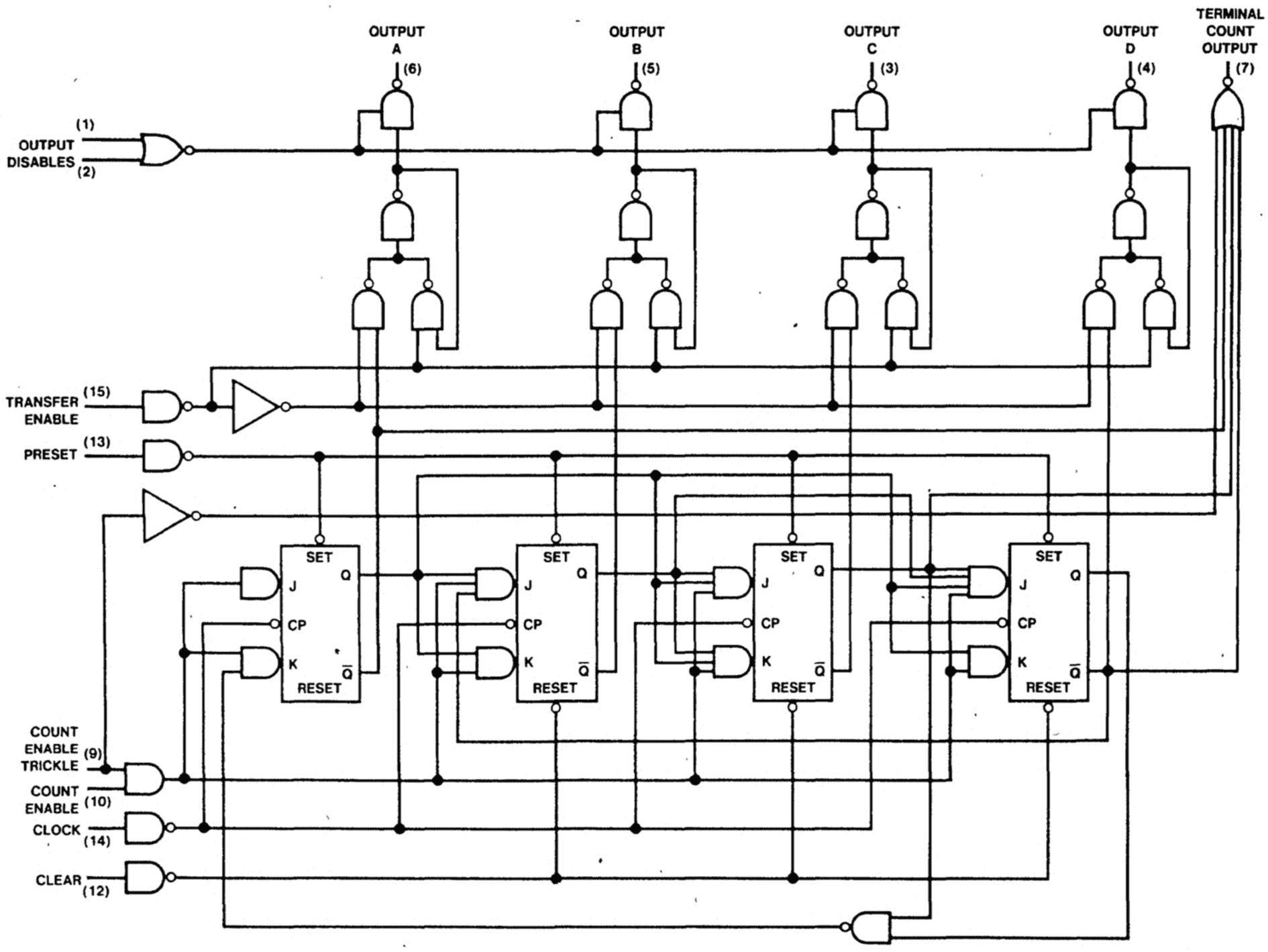
Logic Diagrams

L52



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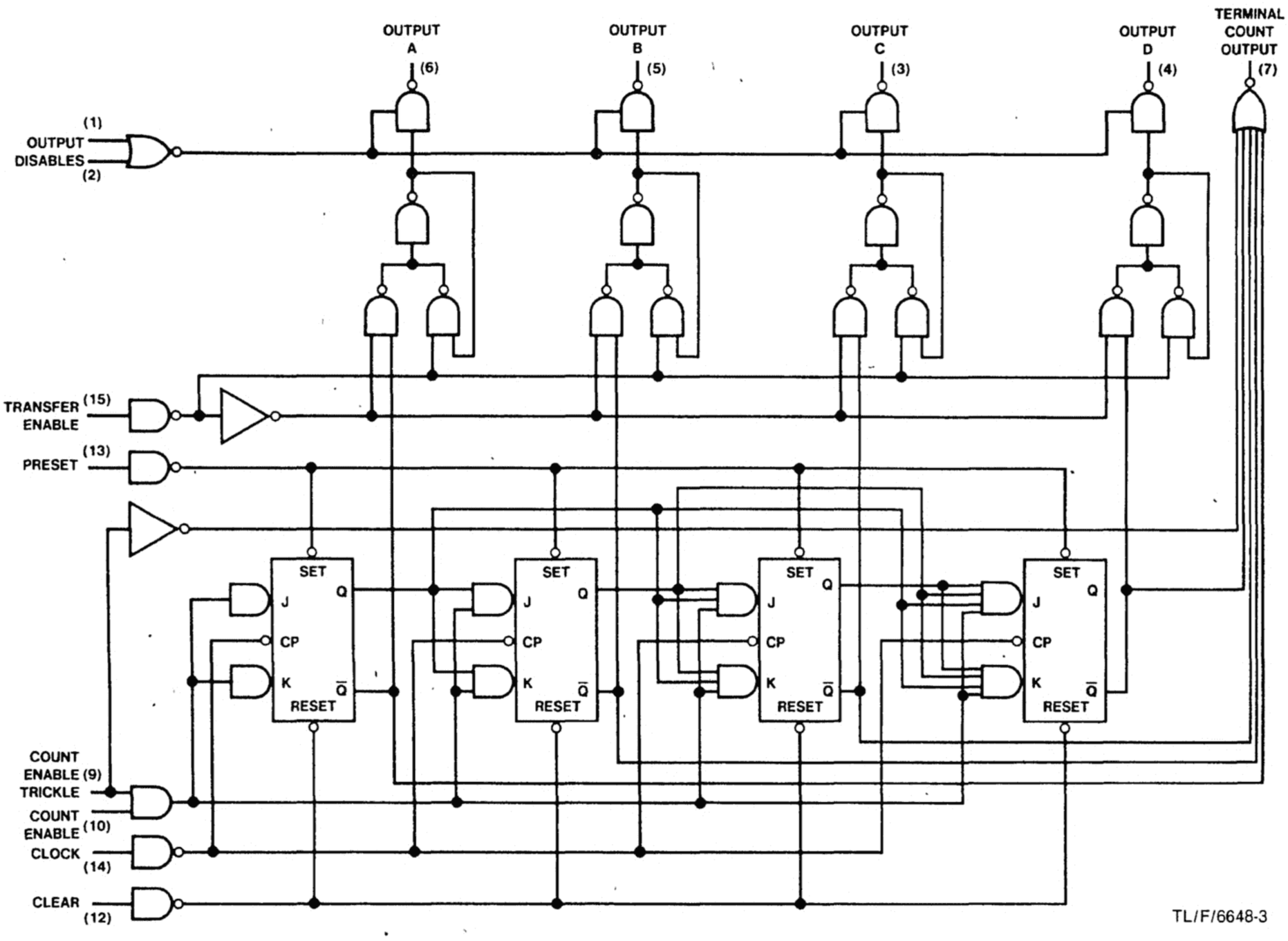
L54



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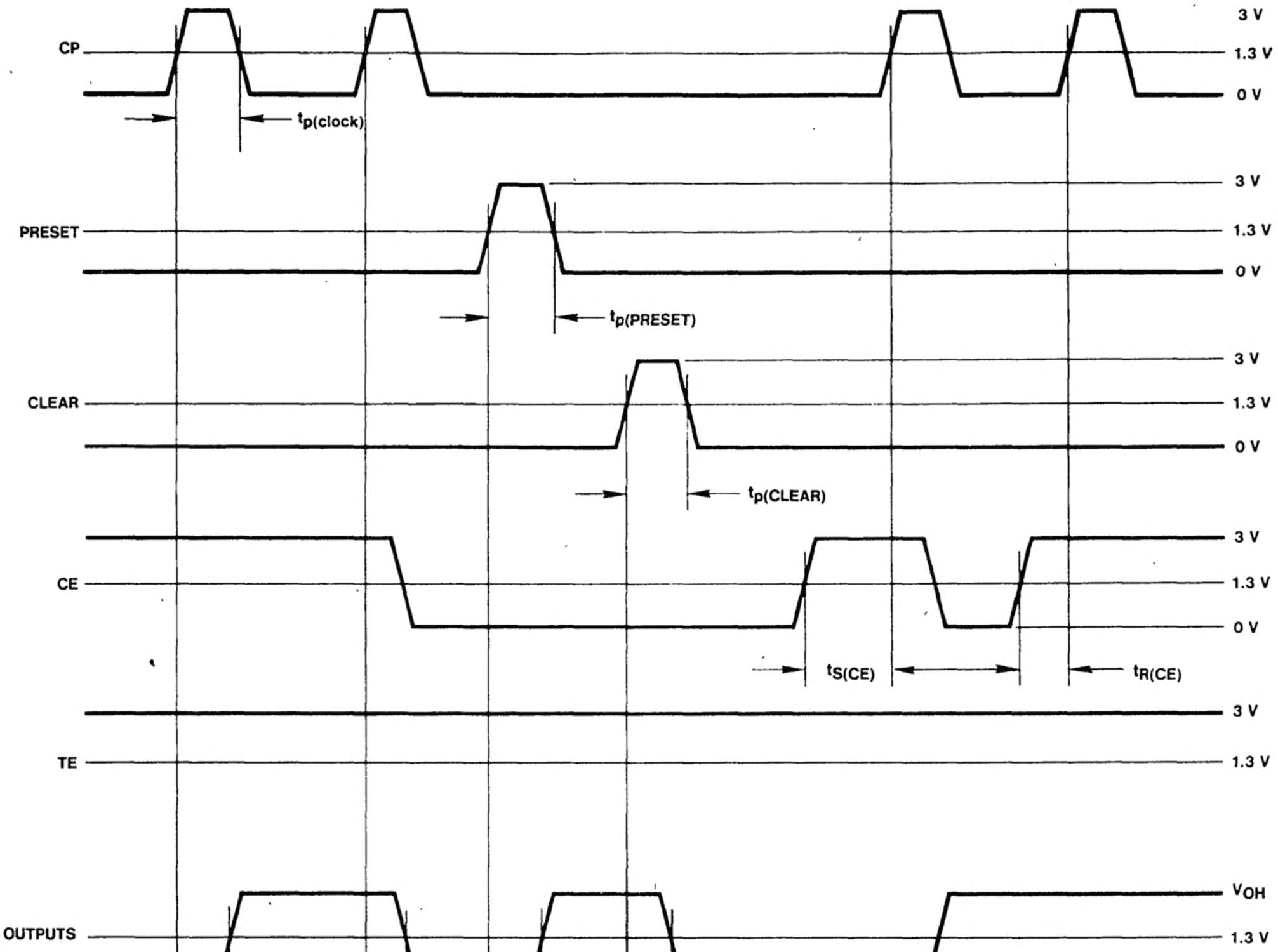
Switching Time Waveforms

L52, L54



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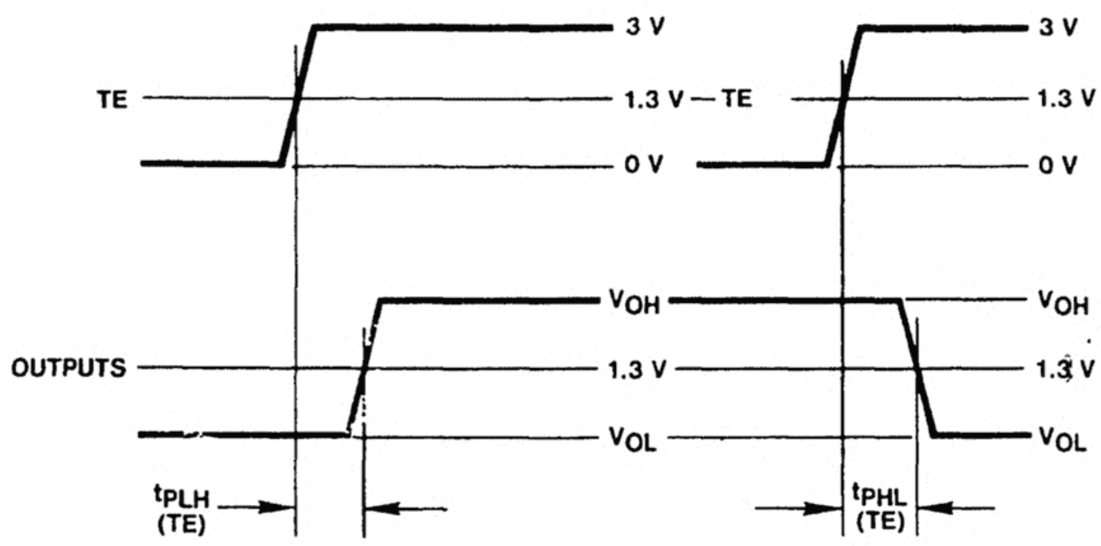

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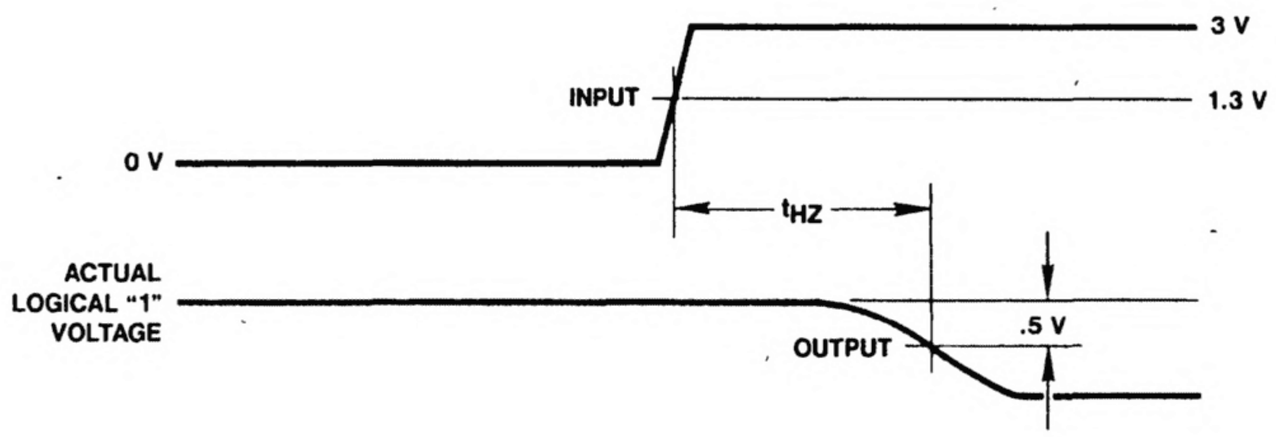
Switching Time Waveforms (Continued)

t_{HZ}



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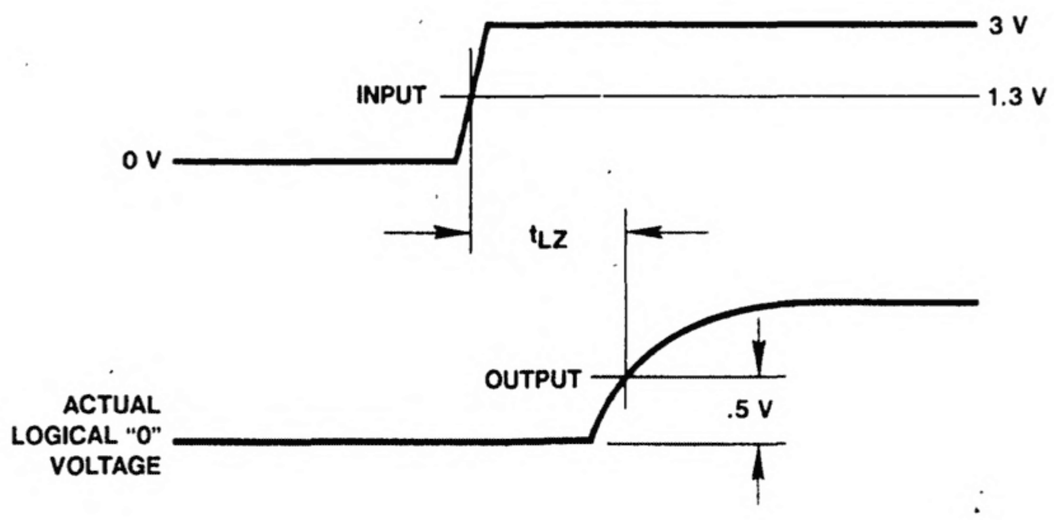
t_{LZ}



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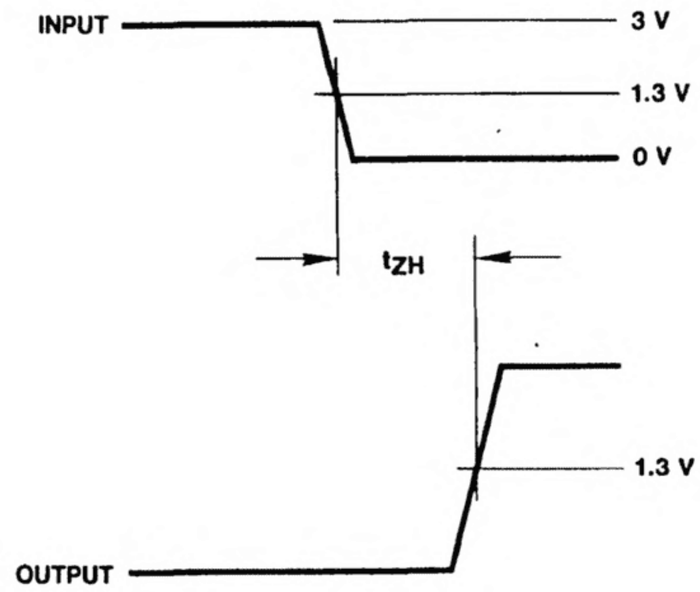
t_{ZH}



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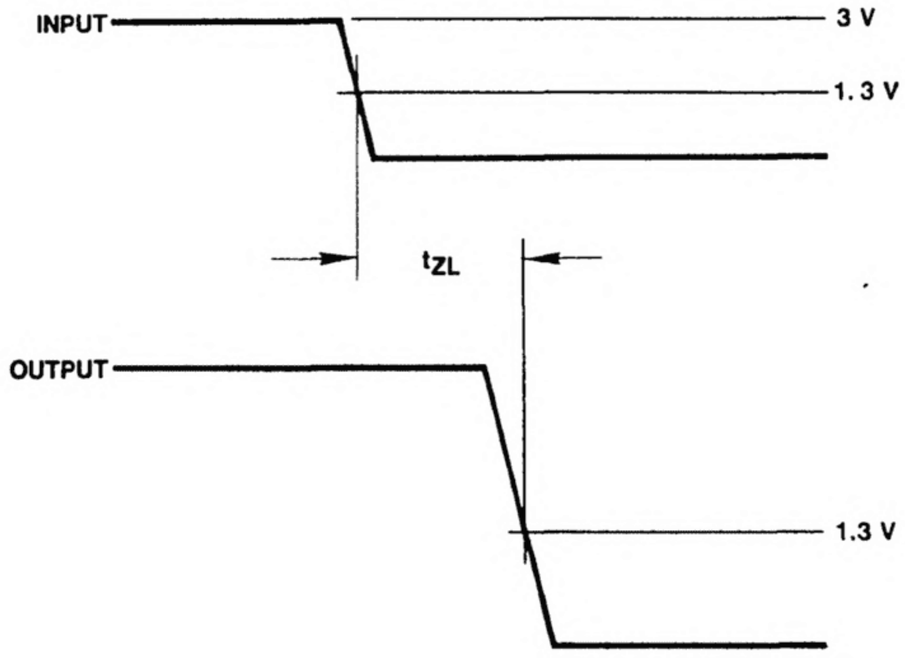
t_{ZL}



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