MUX-16/MUX-28

16-CHANNEL/DUAL 8-CHANNEL JFET ANALOG MULTIPLEXERS (OVERVOLTAGE PROTECTED)

Precision Monolithics Inc.

FEATURES

- **JFET Switches Rather Than CMOS**
- **Highly Resistant To Static Discharge Damage**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 290ΩTypical**
- **Low Leakage Current**
- **Digital Inputs Compatible With TTL and CMOS**
- **Break-Before-Make Action**
- **125° C Temperature-Tested Dice Available**
- **Overvoltage Protected**
- **Supply Loss Protection**
- **MUX-16 Pin Compatible With DG506, HI-506A, AD7506**
- **MUX-28 Pin Compatible With DG507, HI-507A, AD7507**
- **Available in Die Form**

ORDERING INFORMATION †

25°C RESISTANCE	PACKAGE: CERDIP 28-PIN	PACKAGE: LCC 28-CONTACT	PACKAGE: PLASTIC 28-PIN	OPERATING TEMPERATURE RANGE
290Ω	MUX16AT*	–	–	MIL
290Ω	MUX16ET	–	–	IND
400Ω	MUX16BT*	MUX16BTC/883	–	MIL
400Ω	MUX16FT	–	MUX16FP	XIND
400Ω	–	–	MUX16FPC	XIND
290Ω	MUX28AT*	–	–	MIL
290Ω	MUX28ET	–	–	IND
400Ω	MUX28BT*	MUX28BTC/883	–	MIL
400Ω	MUX28FT	–	MUX28FP	XIND
400Ω	–	–	MUX28FPC	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

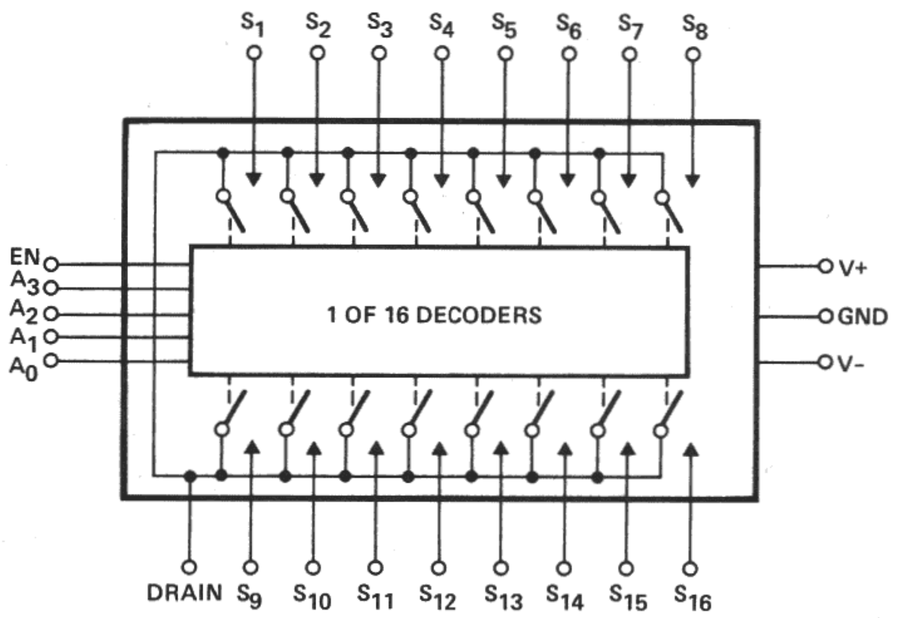
The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

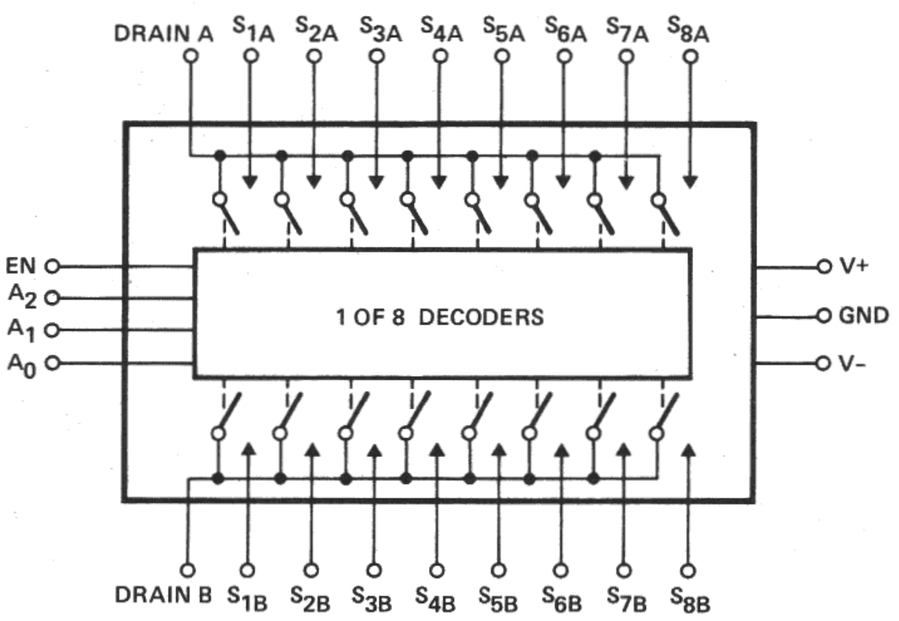
Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

FUNCTIONAL DIAGRAMS

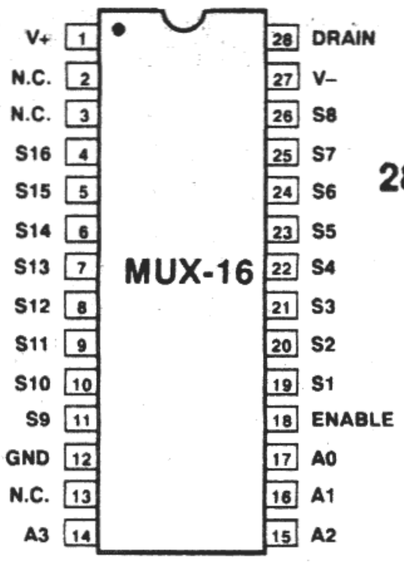
MUX-16



MUX-28

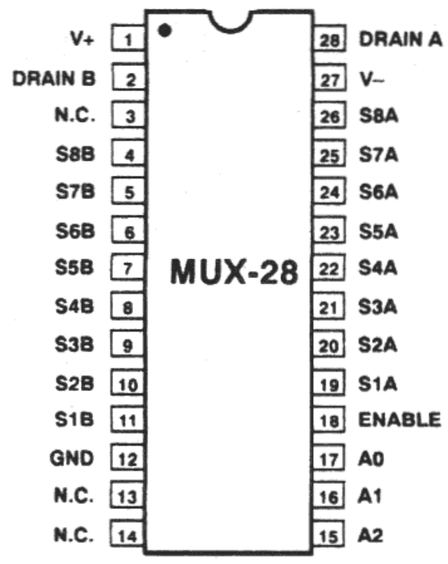


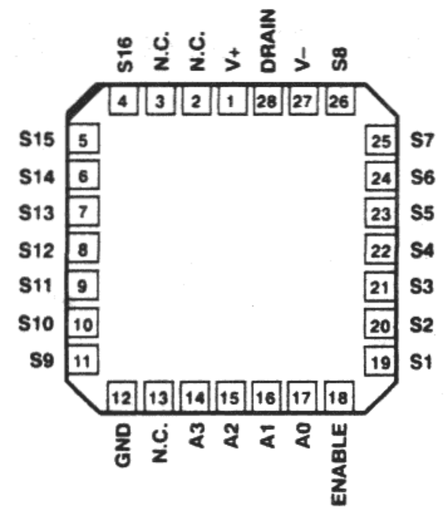
PIN CONNECTIONS & TRUTH TABLES



28-PIN PLASTIC DIP
(P-Suffix)

28-PIN CERDIP
(T-Suffix)





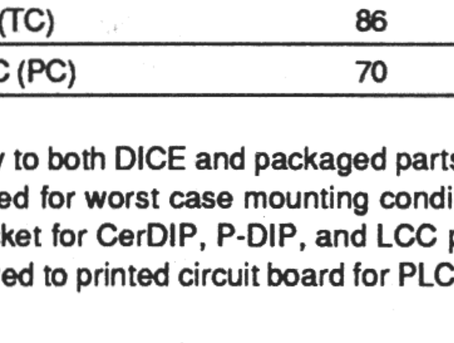
MUX-28BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)

MUX-16

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MUX-28

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8



MUX-16BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range,
- MUX-16/28-AT, BT, BTC ..... –55°C to +125°C
- MUX-16/28-ET ..... –25°C to +85°C
- MUX-16/28-FP, FPC, FT ..... –40°C to +85°C

Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V– Supply 36V
Logic Input Voltage ..... (V– or –4V) to V+ Supply
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{jA} (Note 2)	Θ_{jC}	UNITS
28-Pin Hermetic DIP (T)	55	15	°C/W
28-Pin Plastic DIP (P)	56	30	°C/W
28-Contact LCC (TC)	86	35	°C/W
28-Contact PLCC (PC)	70	33	°C/W

NOTES:
1. Ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for PLCC package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	290	380	—	400	580	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1.5	5	—	1.5	5	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Source Current (Switch "OFF")	I_S (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1	—	0.01	2	nA
Drain Current (Switch "OFF")	I_D (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Leakage Current (Switch "ON")	I_D (ON) $+I_S$ (ON)	$V_D = 10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = +25°C, unless otherwise noted. *Continued*

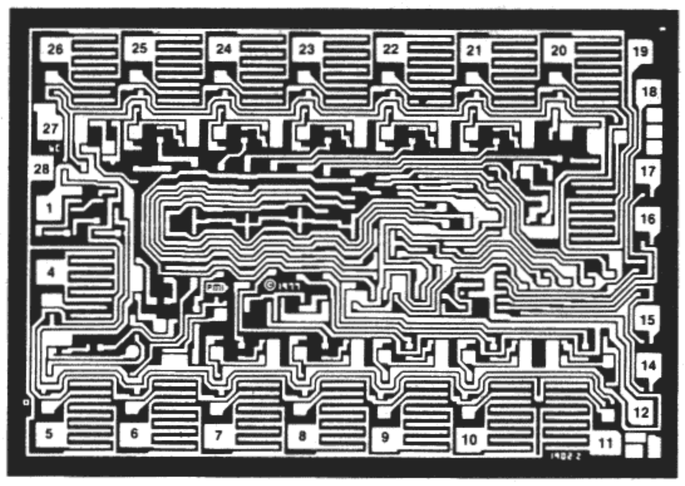
PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V		–	4	10	–	4	10	µA
Digital Input Capacitance	C_{DIG}			–	3	–	–	3	–	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2,5) Figure 1 (Test Circuits)		– –	1.4 1.2	2.0 1.8	– –	1.8 1.6	2.5 2.2	µs
Output Settling Time	t_s	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		– – –	2.6 3.2 4.0	– – –	– – –	2.7 3.4 7.2	– – –	µs
Break-Before-Make Delay	t_{OPEN}	Figure 3		–	0.7	–	–	1	–	µs
Enable Delay "ON"	$t_{ON\ (EN)}$	(Note 5) Figure 2 (Test Circuits)		–	1	2	–	1.2	2.5	µs
Enable Delay "OFF"	$t_{OFF\ (EN)}$	(Note 5) Figure 2 (Test Circuits)	MUX-16 MUX-28	– –	0.25 0.25	0.5 0.5	– –	0.25 0.25	0.5 0.6	µs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 4 (Test Circuits)		–	66	–	–	66	–	dB
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)		–	75	–	–	75	–	dB
Source Capacitance	$C_{S\ (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V		–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D\ (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V	MUX-16 MUX-28	– –	13 8	– –	– –	13 8	– –	pF
Input to Output Capacitance	$C_{DS\ (OFF)}$	(Note 4)		–	0.15	–	–	0.15	–	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 15V V+ = 5V V+ = 5V	MUX-16 MUX-28 MUX-16 MUX-28	– – – –	15 15 12 12	19 19 – –	– – – –	9 8 8 7	19 19 – –	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I–	V– = –15V V– = –15V V– = –5V V– = –5V	MUX-16 MUX-28 MUX-16 MUX-28	– – – –	5 5 4 4	7 7 – –	– – – –	3.5 3 3 2.5	7 7 – –	mA

NOTES:
1. Conditions applied to leakage tests insure worst case leakages.
2. R_L = 10MΩ, C_L = 10pF.
3. Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON. R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for MUX-16AT/BT/BTC and MUX-28AT/BT/BTC; –25°C ≤ T_A ≤ +85°C for MUX-16ET and MUX-28ET; –40°C ≤ T_A ≤ +85°C for MUX-16 FT/FP/FPC and MUX-28FT/FP/FPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S ≤ 10, I_S ≤ 200µA	–	–	500	–	–	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 200µA	–	2	–	–	5.5	–	%
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 200µA	–	10	–	–	15	–	%
Analog Voltage Range	V_A	(Note 6)	+10 –10	+11 –15	– –	+10 –10	+11 –15	– –	V
Source Current (Switch"OFF")	$I_{S\ (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	25	–	–	50	nA
Drain Current (Switch "OFF")	$I_{D\ (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	75	–	–	250	nA
Leakage Current (Switch "ON")	$I_{D\ (ON)}$ $+I_{S\ (ON)}$	V_D = 10V (Note 1)	–	–	75	–	–	250	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	–	–	2	–	–	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	–	–	0.7	–	–	0.7	V
Digital Input Current	I_{IN}	V_{IN} = 0.4V to 15V	–	–	20	–	–	20	µA
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V	–	–	20	–	–	20	µA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	–	–	24	–	–	24	mA
Negative Supply Current	I–	All Digital Inputs Logic "0" or "1"	–	–	8.2	–	–	8.2	mA

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



MUX-16

DIE SIZE 0.110 × 0.076 inch, 8360 sq. mils
(2.794 × 1.930 mm, 5392 sq. mm)

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

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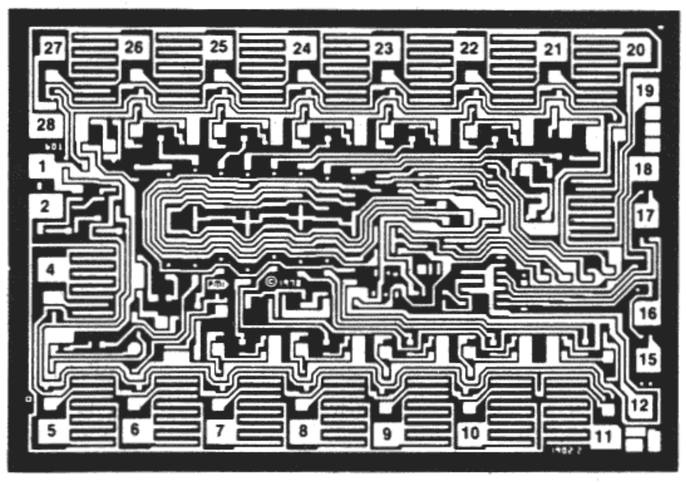


1. POSITIVE SUPPLY
4. SOURCE 16 (S16)
5. SOURCE 15 (S15)
6. SOURCE 14 (S14)
7. SOURCE 13 (S13)
8. SOURCE 12 (S12)
9. SOURCE 11 (S11)
10. SOURCE 10 (S10)
11. SOURCE 9 (S9)
12. GROUND
14. ADDRESS BIT 3 (A3)
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1)
20. SOURCE 2 (S2)
21. SOURCE 3 (S3)
22. SOURCE 4 (S4)
23. SOURCE 5 (S5)
24. SOURCE 6 (S6)
25. SOURCE 7 (S7)
26. SOURCE 8 (S8)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN

1. POSITIVE SUPPLY
2. DRAIN B
4. SOURCE 8 (S8B)
5. SOURCE 7 (S7B)
6. SOURCE 6 (S6B)
7. SOURCE 5 (S5B)
8. SOURCE 4 (S4B)
9. SOURCE 3 (S3B)
10. SOURCE 2 (S2B)
11. SOURCE 1 (S1B)
12. GROUND
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1A)
20. SOURCE 2 (S2A)
21. SOURCE 3 (S3A)
22. SOURCE 4 (S4A)
23. SOURCE 5 (S5A)
24. SOURCE 6 (S6A)
25. SOURCE 7 (S7A)
26. SOURCE 8 (S8A)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN A

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C for MUX-16/28 N and G, T_A = 125°C for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 200μA	540	380	800	580	Ω MAX
Digital "1" Input Voltage	V_{INH}		2	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V	20	10	20	10	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.4V	20	10	20	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−		8.2	7	8.2	7	mA MAX
Analog Input Range	V_A	(Note 2)	±10	±10	±10	±10	V MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

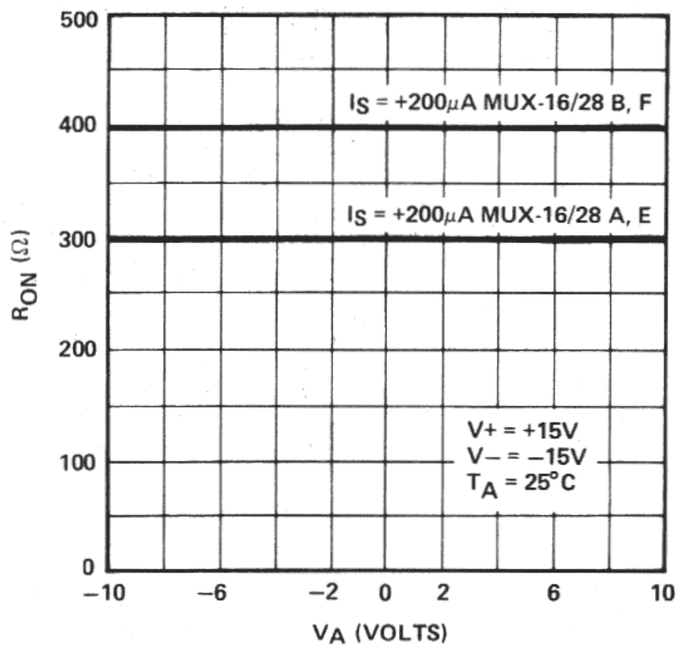
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25°C for MUX-16/28 N and G, T_A = 125°C for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1) Figure 1	2 1.8	1 0.9	2.6 2.4	1.5 1.4	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	CT	(Note 1) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, I_S = 200μA	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 1)	20	0.2	20	0.2	nA
Analog Input Range	V_A	(Note 2)	+11 −15	+11 −15	+11 −15	+11 −15	V

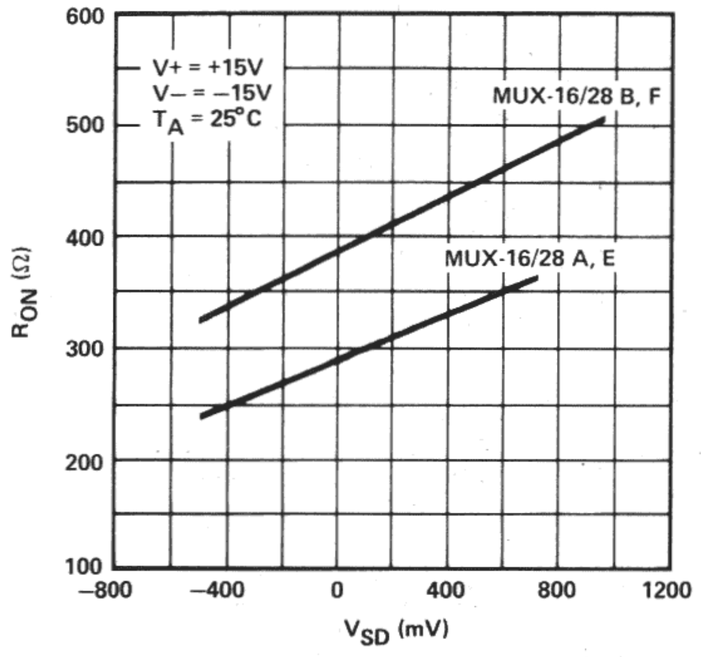
NOTES:
1. The data shown is extrapolated from measurements made on the packaged devices.
2. Guaranteed by R_{ON} and leakage current tests.

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

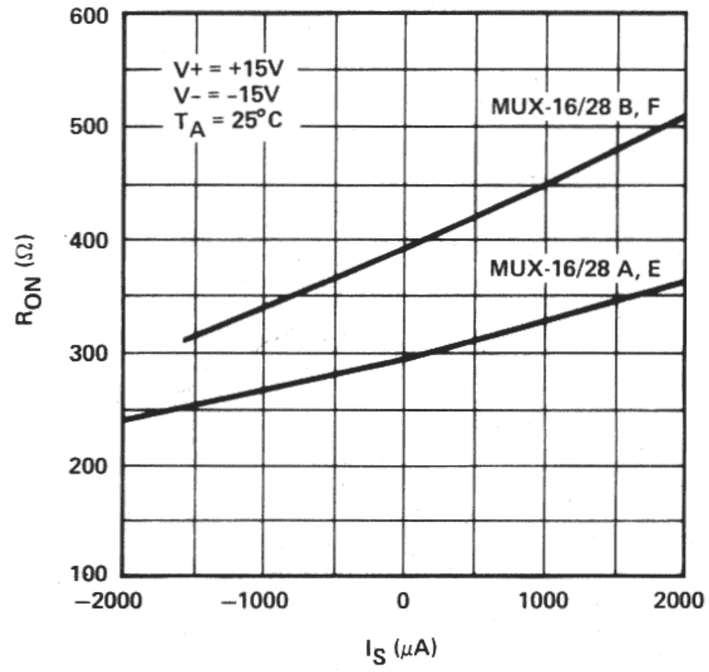
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



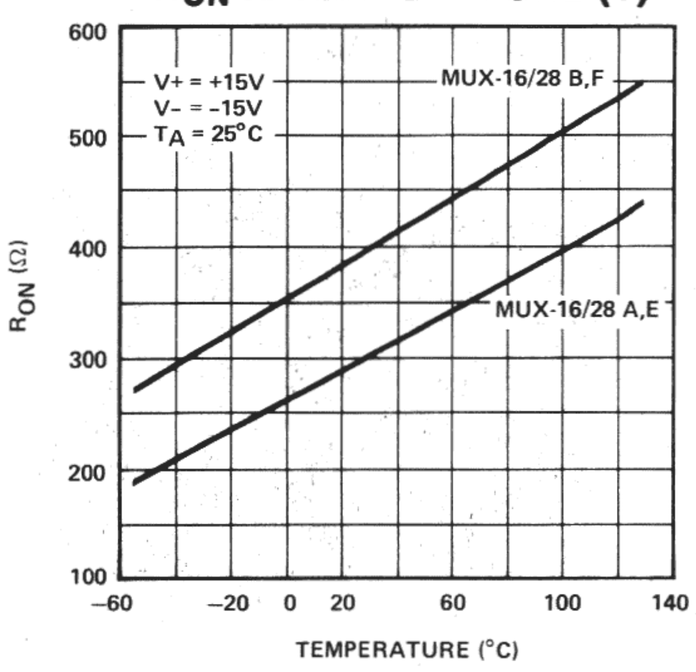
R_{ON} vs SWITCH VOLTAGE (V_{SD})



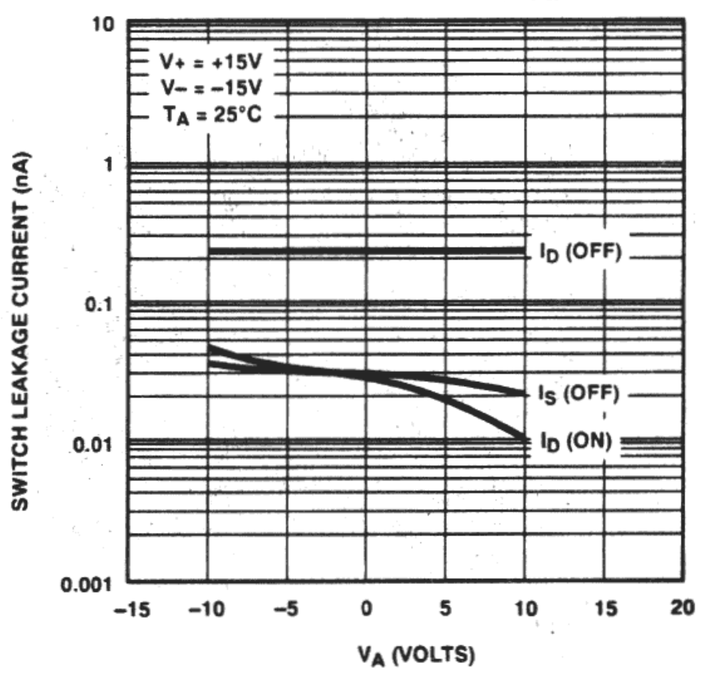
R_{ON} vs SWITCH CURRENT (I_S)



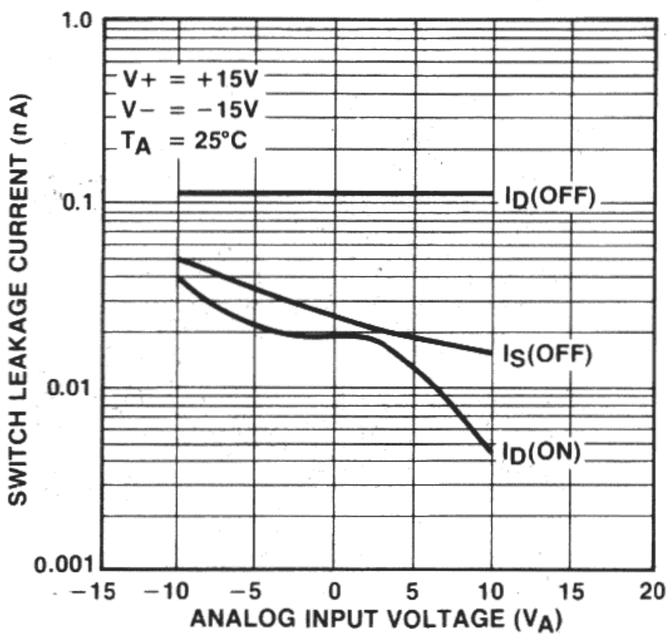
R_{ON} vs TEMPERATURE (T)



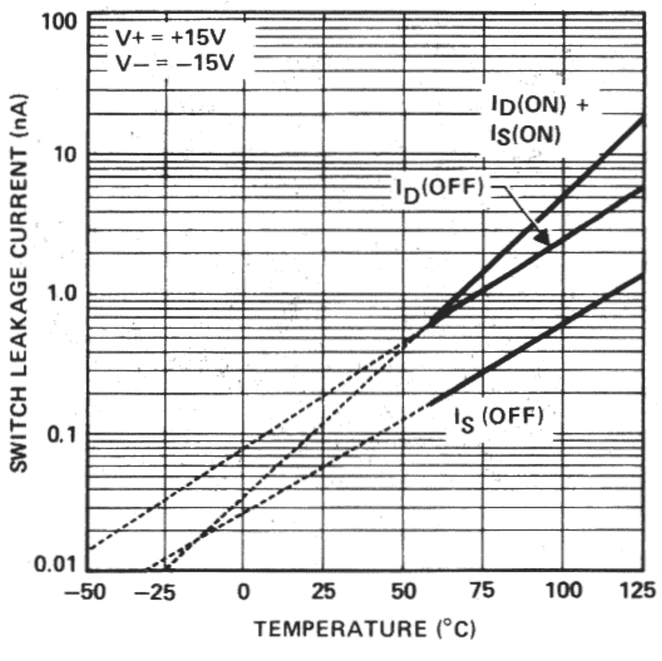
MUX-16 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



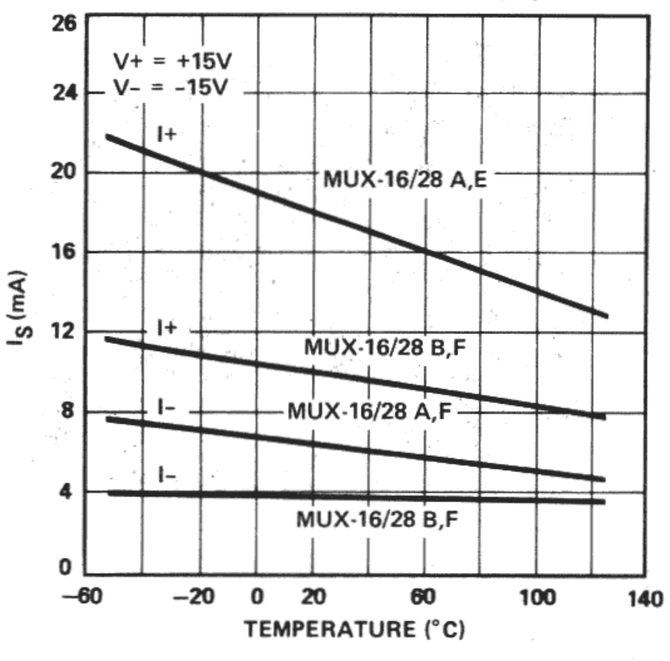
MUX-28 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



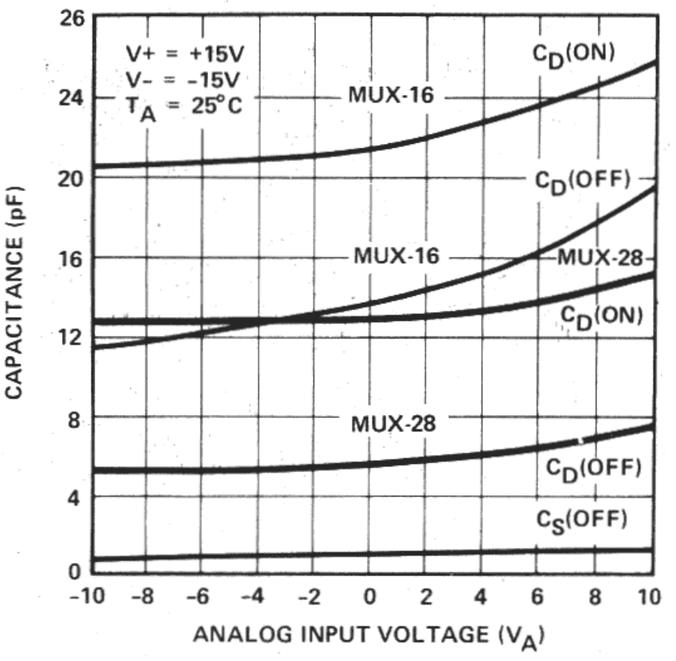
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SUPPLY CURRENTS vs TEMPERATURE (T)

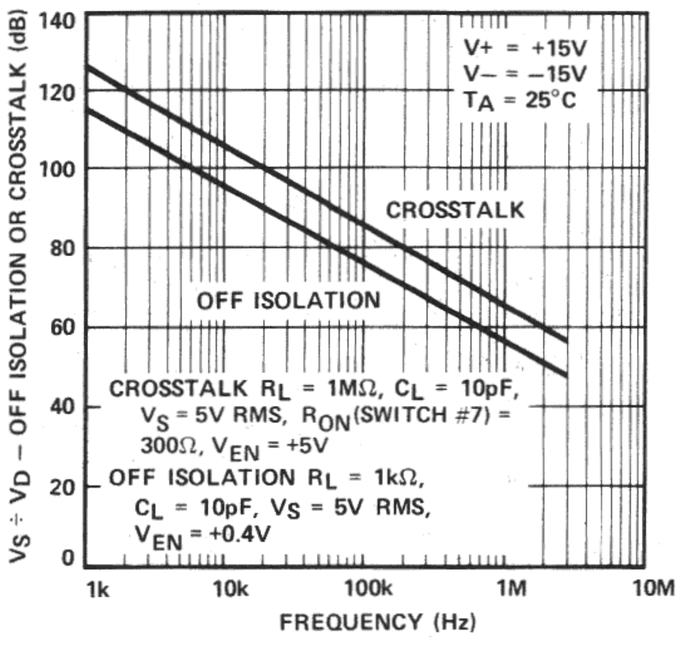


SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)

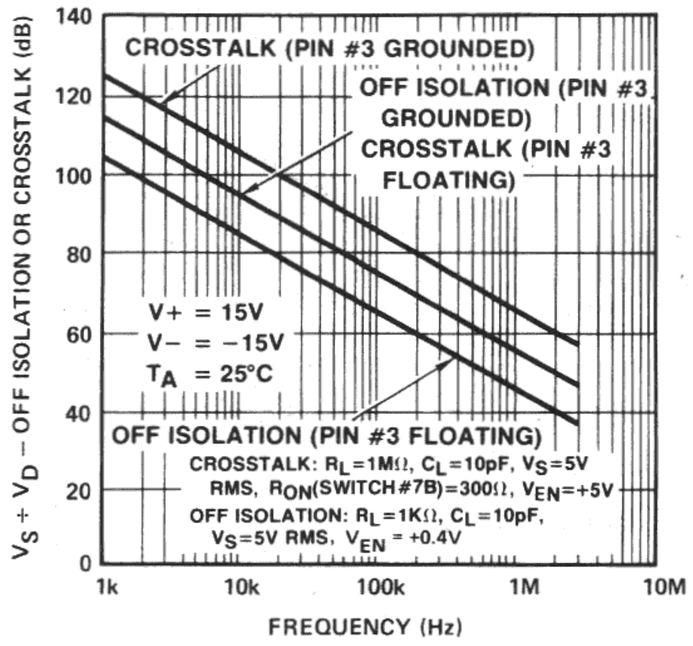


TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

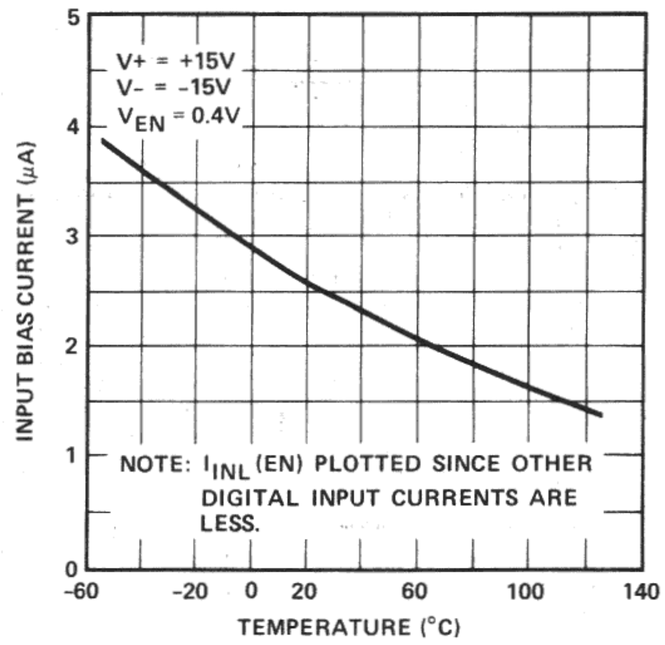
MUX-16 OFF PERFORMANCE OF CHANNEL 8



MUX-28 OFF PERFORMANCE OF CHANNEL 8

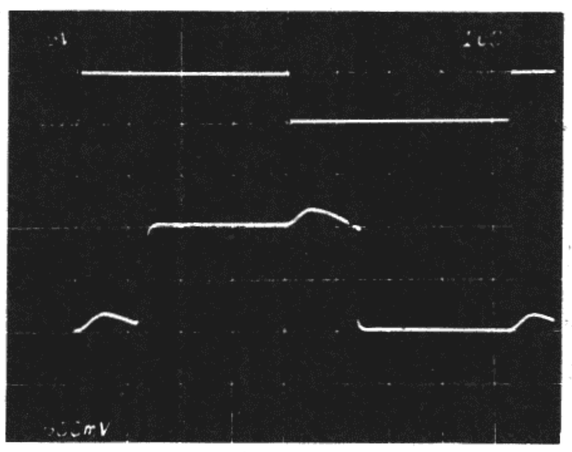


DIGITAL INPUT BIAS CURRENTS vs TEMPERATURE (T)



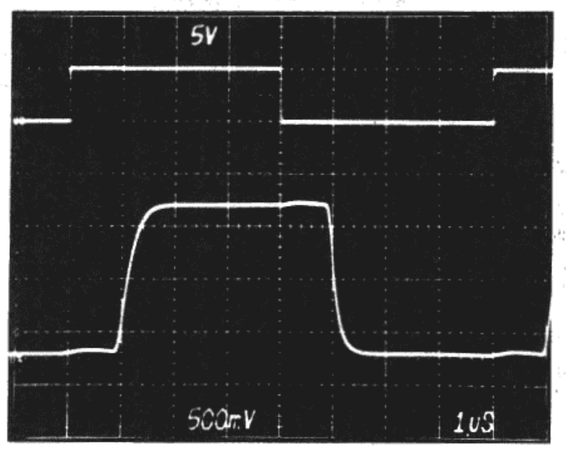
MUX-16 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



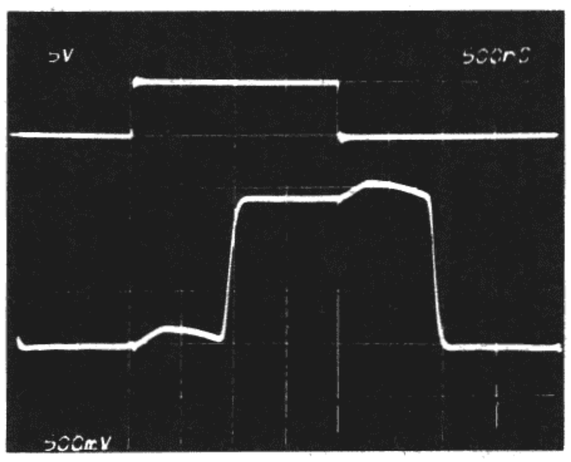
R_L = 1MΩ, C_L = 10pF, V_1 = –500mV, V_{16} = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



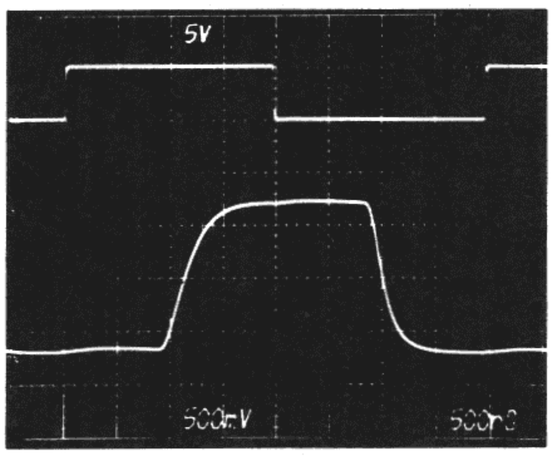
R_L = 1MΩ, C_L = 500pF, V_1 = –500mV, V_{16} = +500mV

SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME



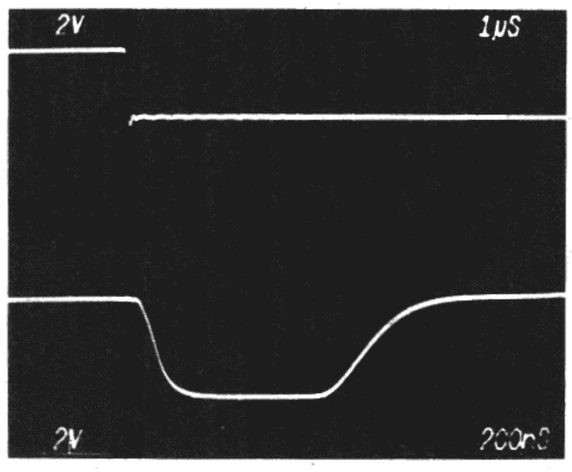
R_L = 1MΩ, C_L = 10pF, V_1 = –700mV, V_{16} = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2μs SAMPLE TIME



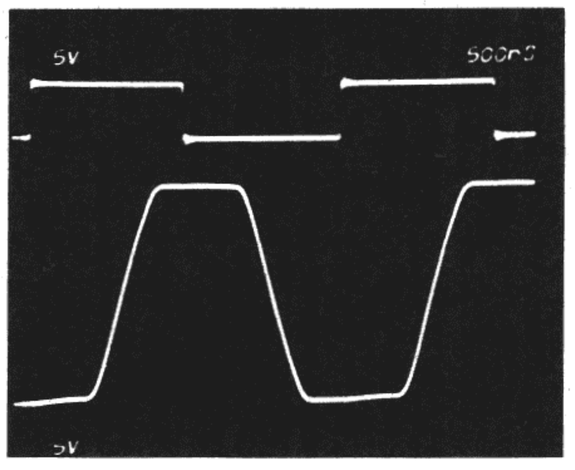
R_L = 1MΩ, C_L = 500pF, V_1 = –700mV, V_{16} = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1kΩ, C_L = 10pF, V_1 = V_{16} = +10V

LARGE-SIGNAL SWITCHING

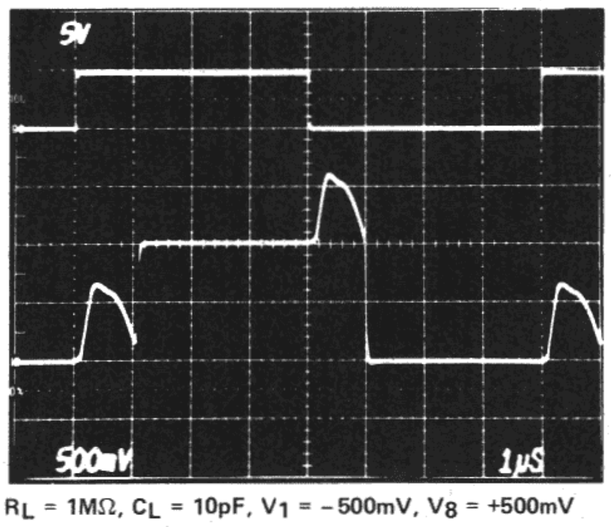


R_L = 1MΩ, C_L = 10pF, V_1 = –10V, V_{16} = +10V

NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

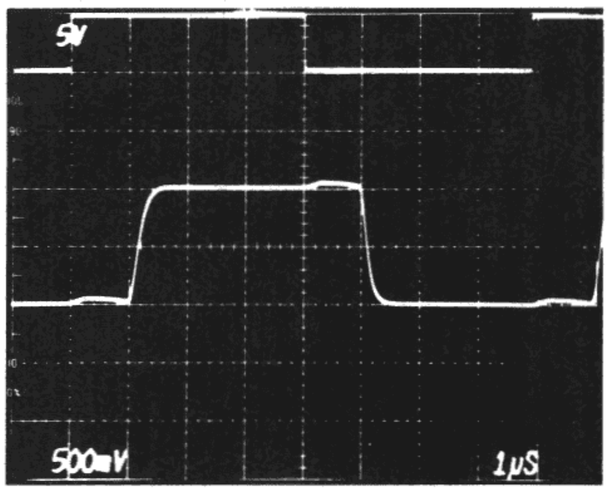
MUX-28 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



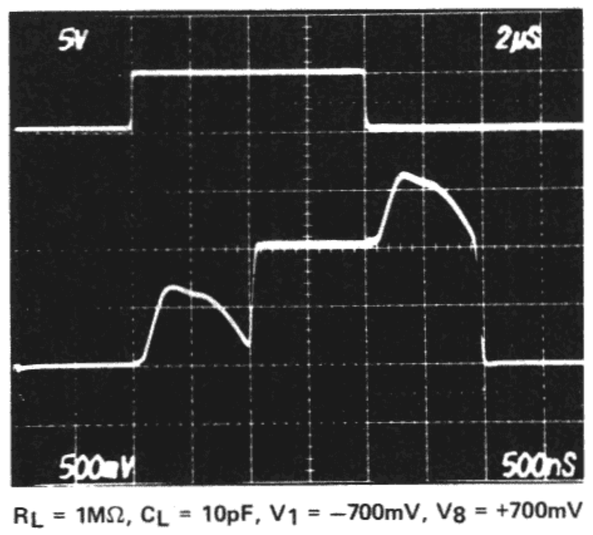
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



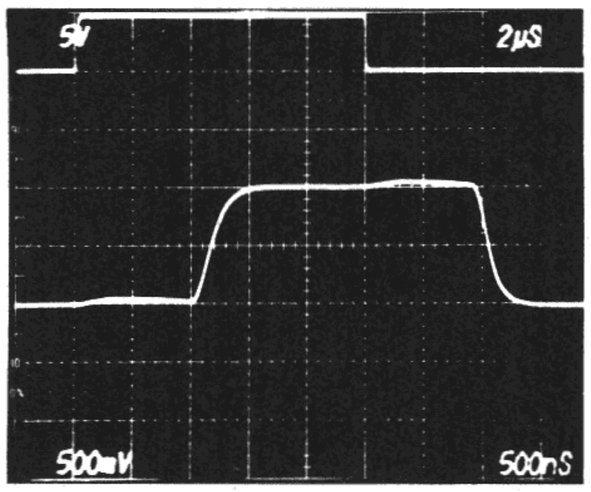
R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



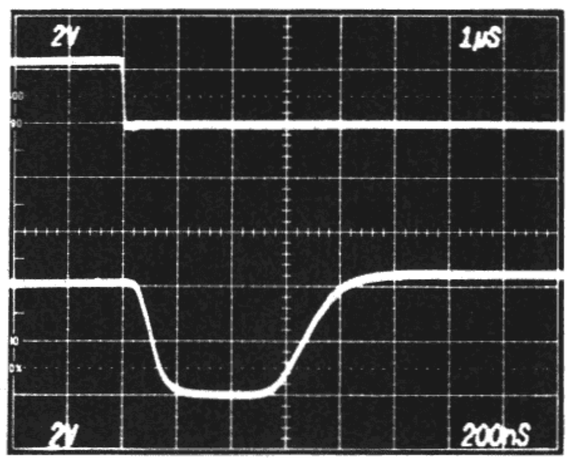
R_L = 1MΩ, C_L = 10pF, V_1 = −700mV, V_8 = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



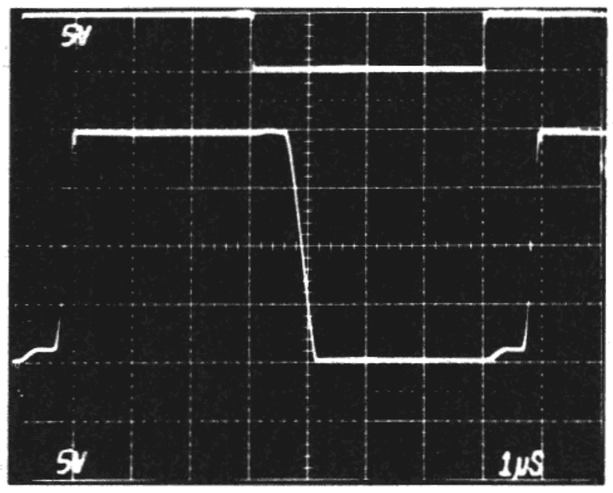
R_L = 1MΩ, C_L = 500pF, V_1 = −700mV, V_8 = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1KΩ, C_L = 10pF, V_1 = V_8 = +10V

LARGE-SIGNAL SWITCHING

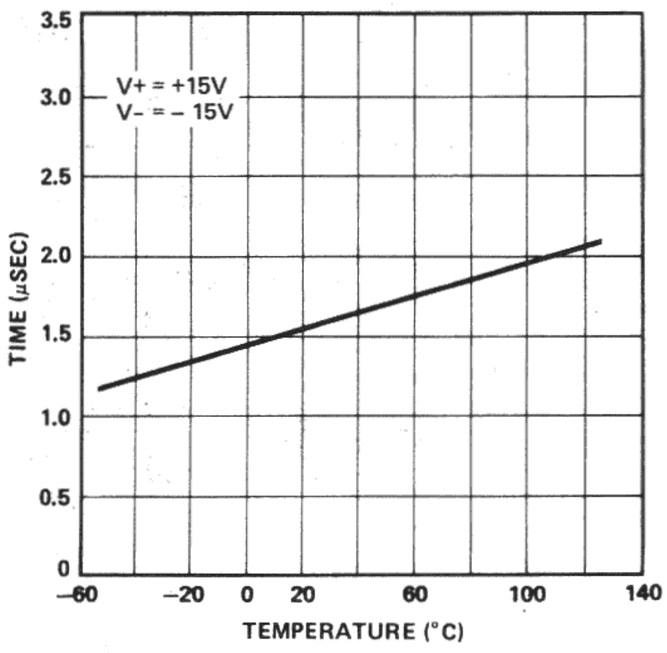


R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V

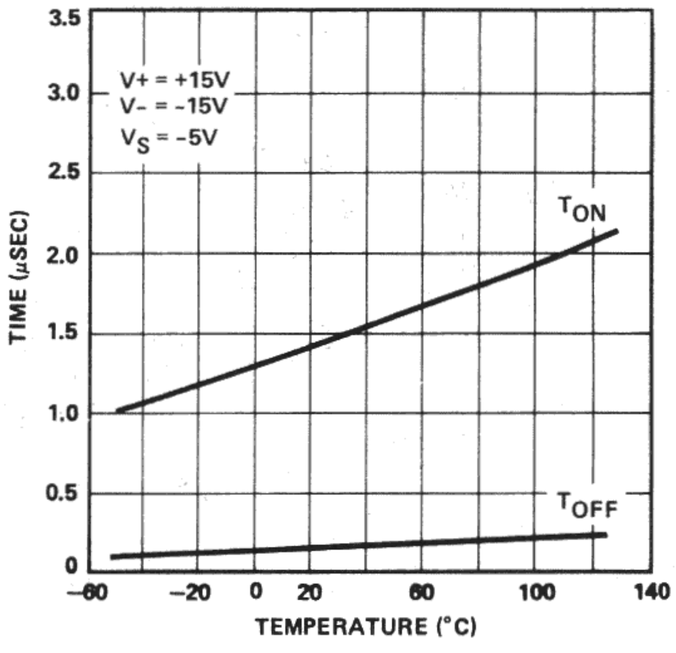
NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

TRANSITION TIME vs TEMPERATURE

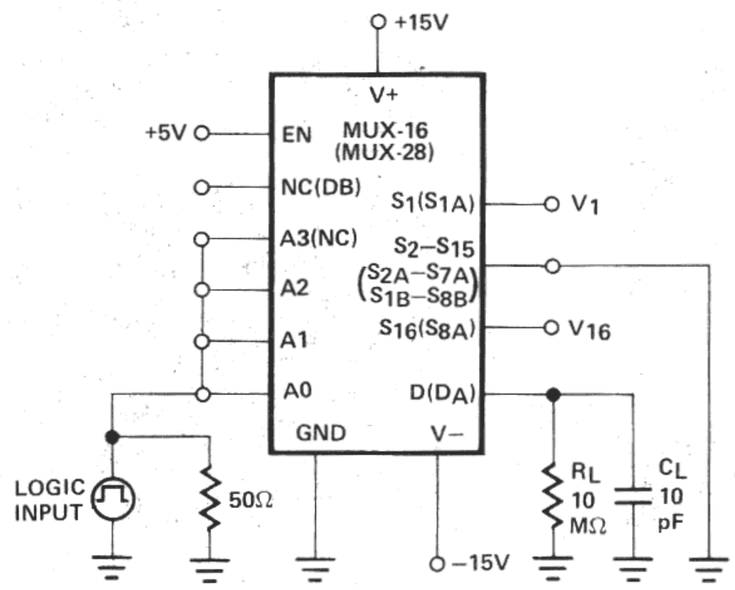


ENABLE DELAY TIME vs TEMPERATURE



A.C. TEST CIRCUITS

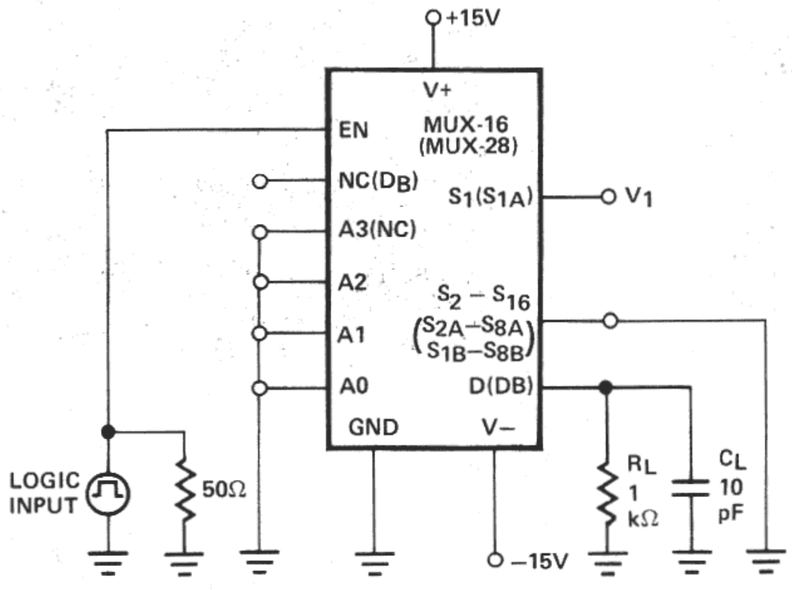
TRANSITION TIME TEST CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

Figure 1

ENABLE DELAY TIME TEST CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

Figure 2

BREAK-BEFORE-MAKE TEST CIRCUIT

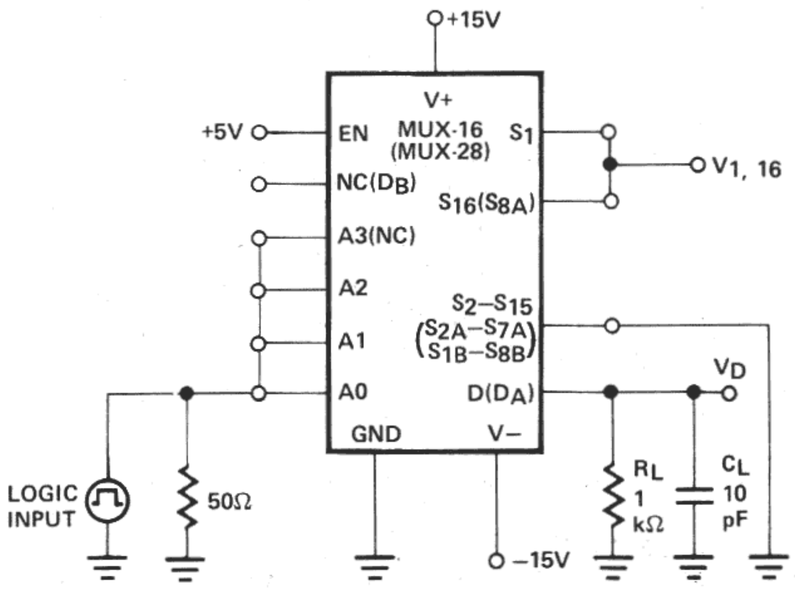
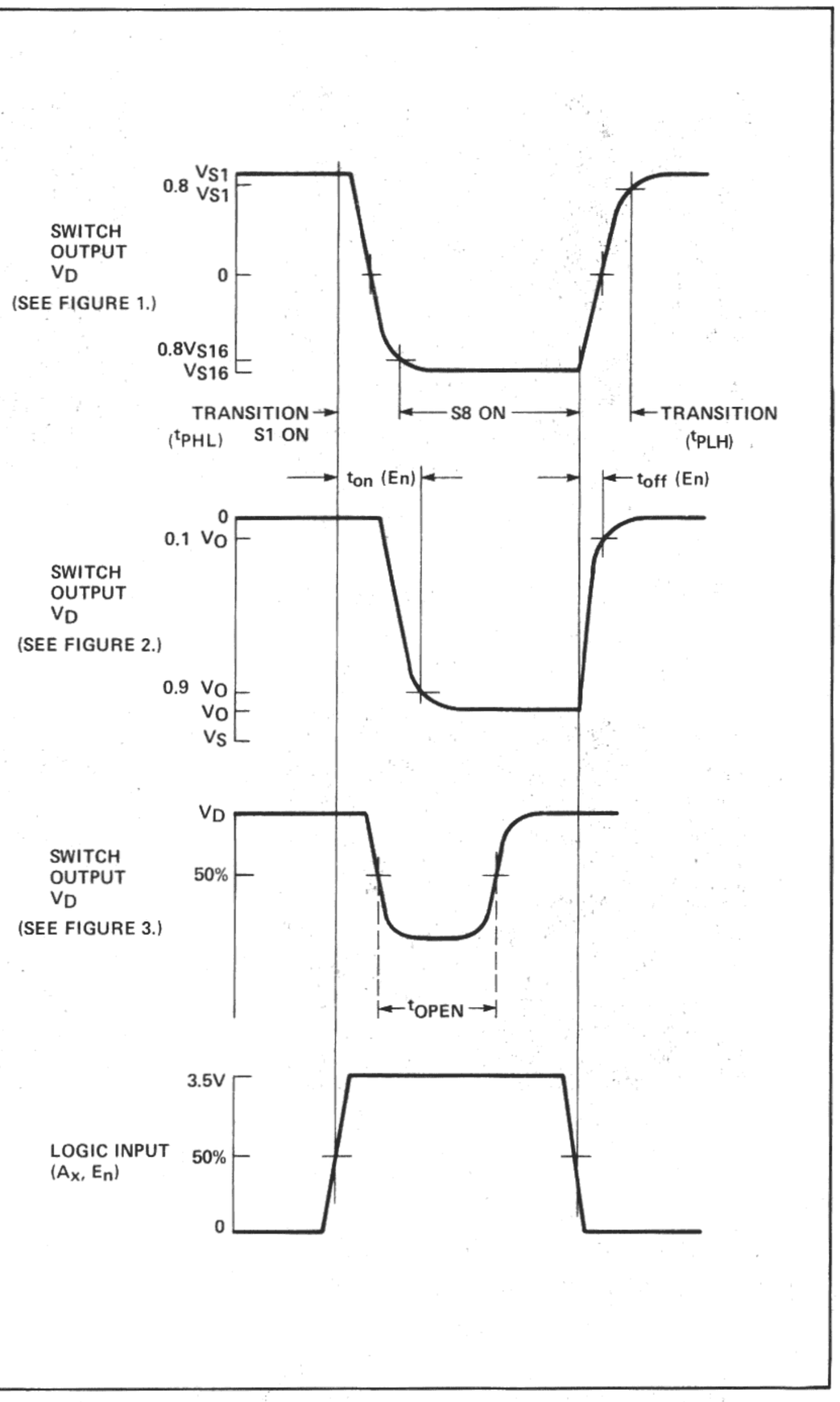


Figure 3 ( ) DENOTES MUX-28 CONNECTIONS

SWITCHING TIME WAVEFORMS



OFF ISOLATION TEST CIRCUIT

$$ISO_{OFF} = 20 \log \frac{|V_S|}{|V_D|}$$

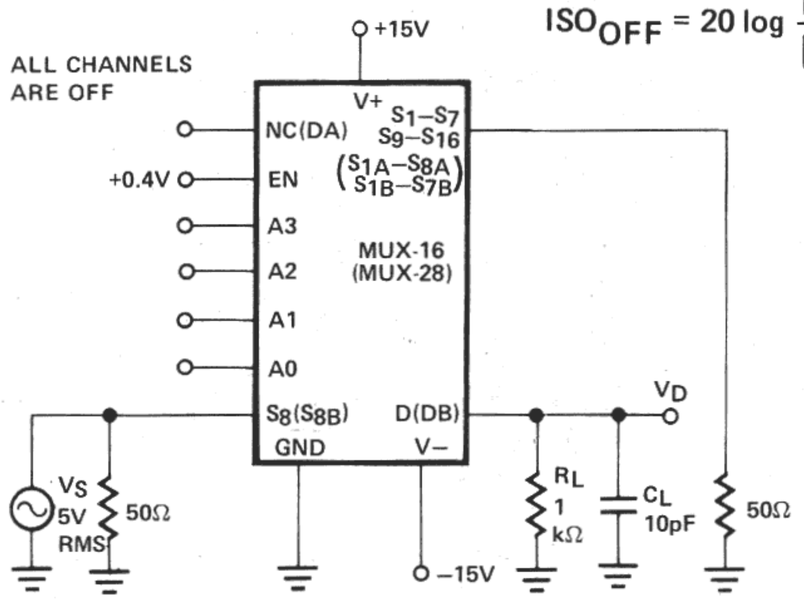
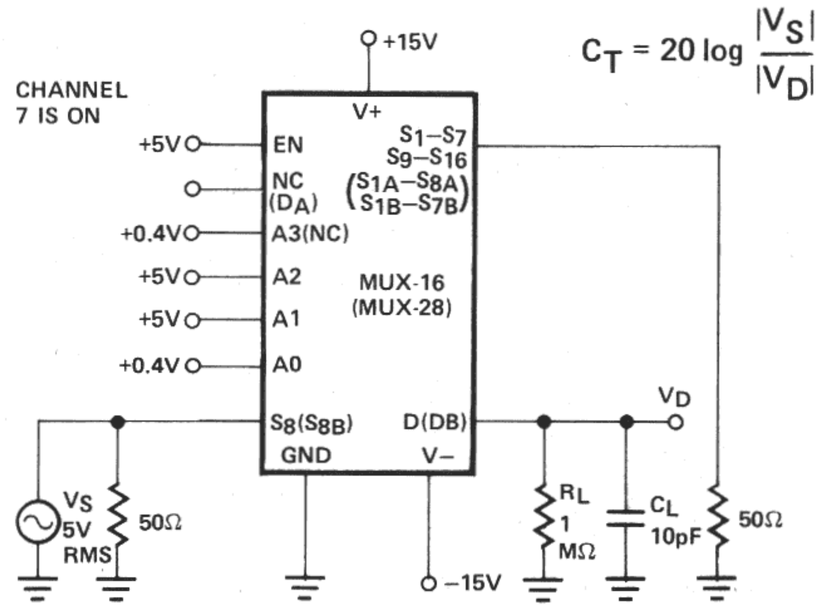


Figure 4 ( ) DENOTES MUX-28 CONNECTIONS

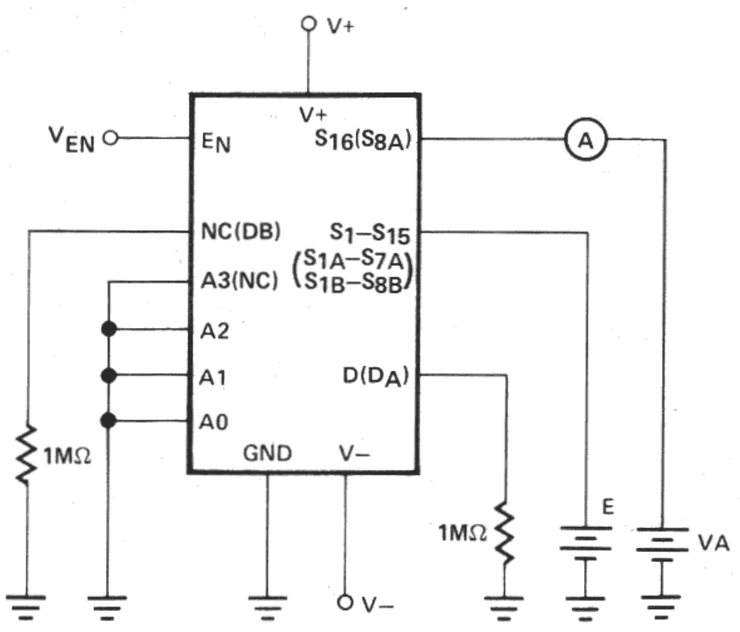
CROSSTALK MEASUREMENT CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

Figure 5

OVERVOLTAGE MEASUREMENT TEST CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

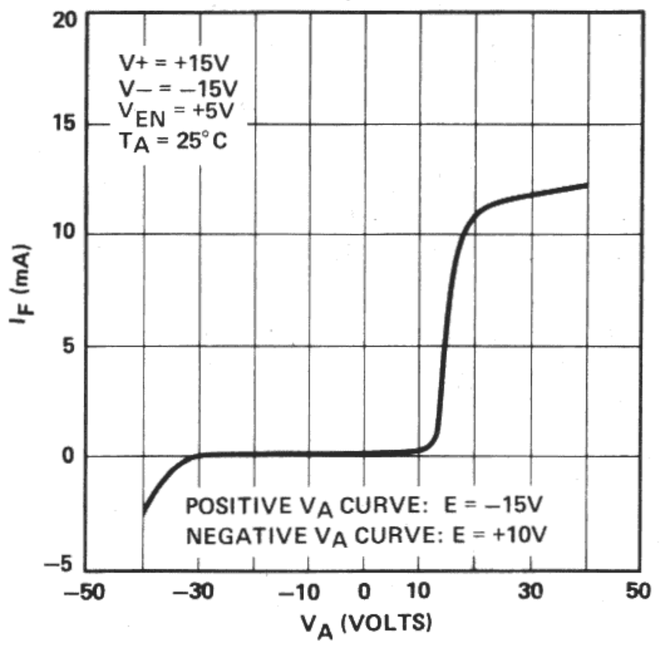
APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with JFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

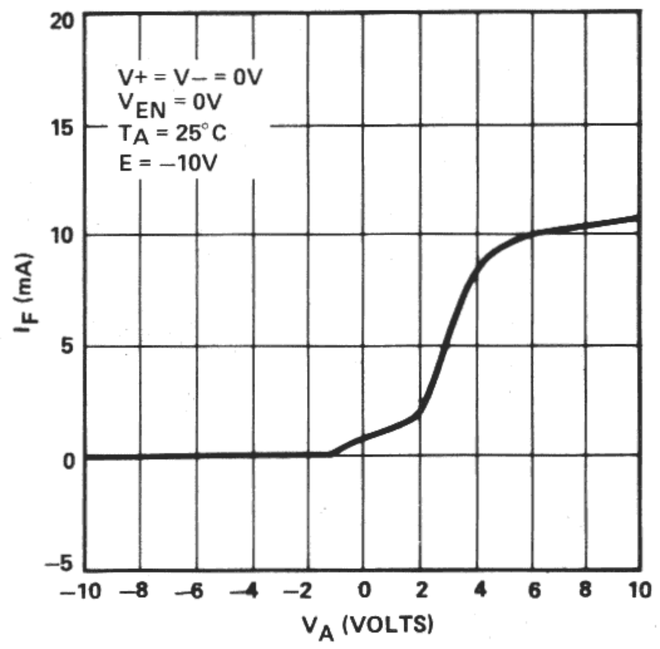
The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF FET switch remains greater than its V_P, preventing that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μSec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

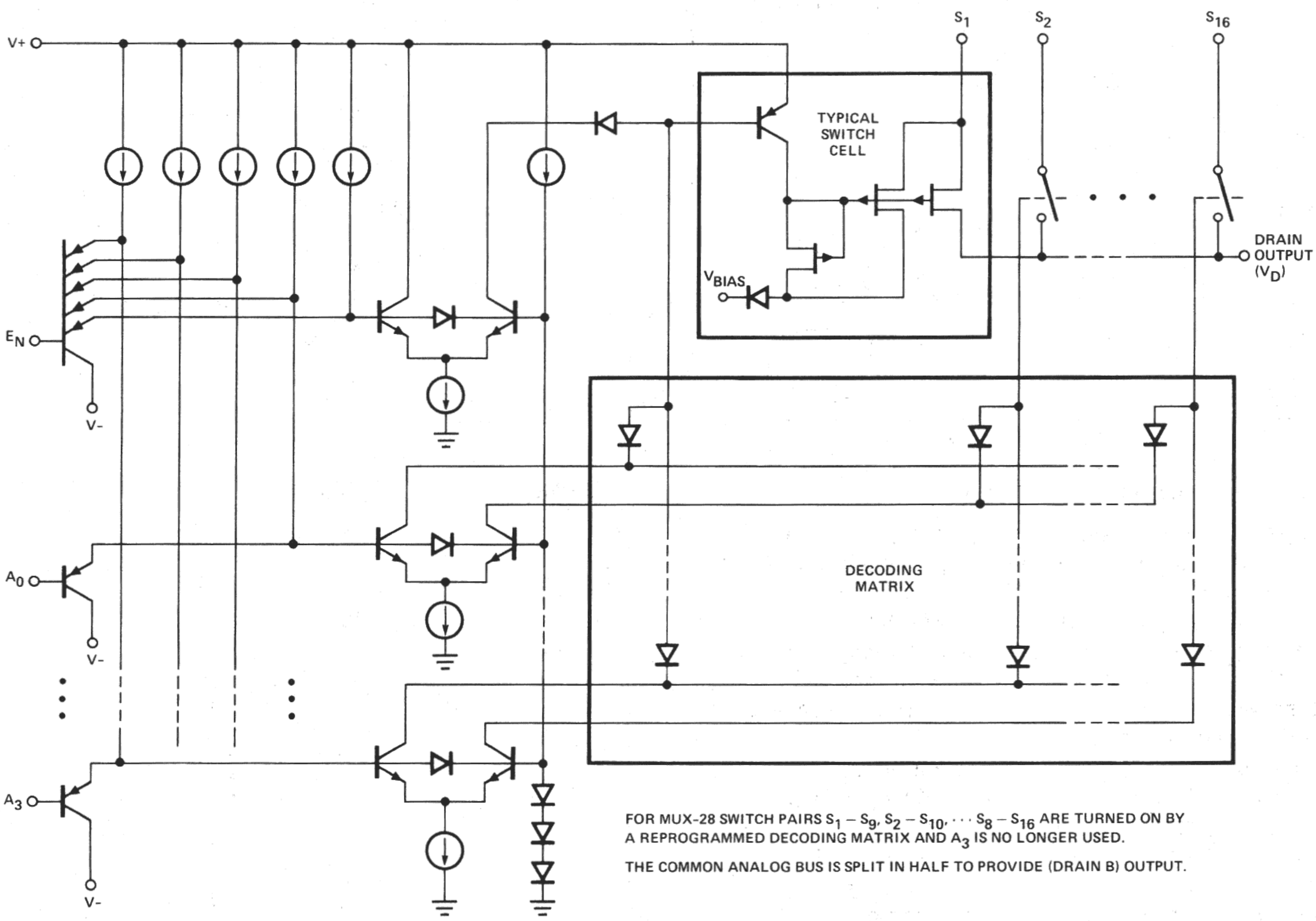
OVERVOLTAGE V-I CHARACTERISTIC



SUPPLY-LOSS V-I CHARACTERISTIC



SIMPLIFIED SCHEMATIC (MUX-16)



FOR MUX-28 SWITCH PAIRS $S_1 - S_9$, $S_2 - S_{10}$, $\cdots$ $S_8 - S_{16}$ ARE TURNED ON BY A REPROGRAMMED DECODING MATRIX AND A_3 IS NO LONGER USED.

THE COMMON ANALOG BUS IS SPLIT IN HALF TO PROVIDE (DRAIN B) OUTPUT.

INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — the bipolar-JFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low "R_{ON}" resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent "R_{ON}" may typically be over 1000 ohms.

JFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low "R_{ON}" resistance. In addition, the special handling required with CMOS devices is not necessary with JFET switches.

In selecting analog multiplexers, attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by "R_{ON}" resistance and "C_{OUT}" capacitance specifications. A low "R_{ON}" insures minimum signal attenuation and maximum accuracy. The "C_{OUT}" capacitance forms on R-C time constant with "R_{ON}" placing fundamental limits on signal acquisition time. Low "R_{ON}" and "C_{OUT}" insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

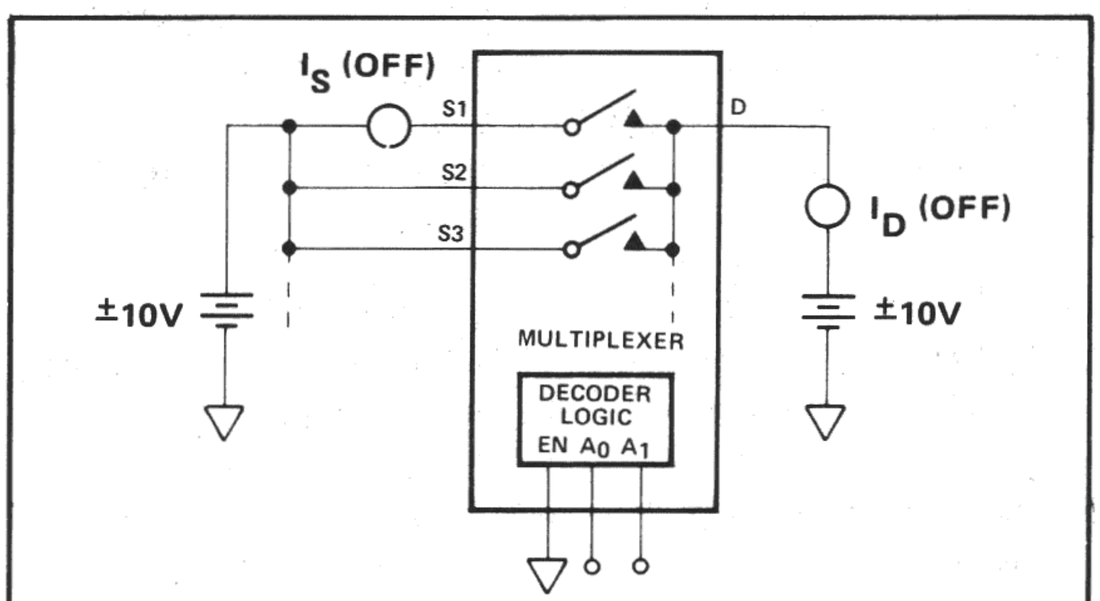
PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

Two new additions to PMI's analog switch product offering are the SSM-2402 and SSM-2412. These dual channel devices provide *click-free* switching in audio applications.

DEFINITIONS

Analog Current Range (I_A, I_S) — The minimum range of currents the switch is capable of conducting in the ON state without degrading ON resistance. It is measured as the value of conduction current that does not cause more than a doubling of the R_{ON} value for the product grade.

$I_{D(OFF)}$, $I_{S(OFF)}$ Test Condition Definitions



NOTES:
1. SWITCHES TURNED "OFF" VIA ENABLE PIN OF DECODER LOGIC FOR I_D (OFF), I_S (OFF) MEASUREMENTS.
2. I_S (OFF) IS TESTED AT EACH INPUT (SOURCE) TERMINAL.

Analog Input Leakage Current ($I_{S(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel source input to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output Leakage Current ($I_{D(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output-To-Input Capacitance ($C_{DS(OFF)}$) — The equivalent capacitance which shunts an open switch effectively between "S" and "D" output.

Analog Input Capacitance ($C_{S(ON)}$) — The capacitance between an analog "S" input and ground with the channel ON.

Analog Input Capacitance ($C_{S(OFF)}$) — The capacitance between an analog "S" input and ground with the channel OFF.

Analog Output Capacitance ($C_{D(OFF)}$) — The capacitance between the analog (DRAIN) output and ground with the channel OFF. High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON}.

Analog Output Capacitance ($C_{D(ON)}$) — The capacitance between the analog "D" output and ground with the channel ON.

Analog Voltage Range (V_A) — The range of analog-voltage amplitudes, with-respect-to ground, over which the analog switch operates (ON/OFF) within the R_{ON} and leakage specifications — $I_{S(OFF)}$, $I_{D(OFF)}$ and $I_{D(ON)} + I_{S(ON)}$.

Break-Before-Make Delay (t_{OPEN}) — The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance ($C_{SS(OFF)}$, $C_{DD(OFF)}$) — The capacitance between the D(S) terminals of any two channels.

Charge Transfer (Q) — Charge transfer appears as a voltage step (pedestal) on the output capacitor after switch turn OFF. The undesirable charge AC couples directly from the logic-control driver to the switch contact.

Crosstalk (CT) — The proportionate amount of cross-coupling from an analog input channel to another output channel, expressed in dB.

Digital Input Capacitance (C_{DIG}) — The capacitance between a digital input and ground.

Insertion Loss — Insertion loss measures the amount of signal power absorbed by the switch ON resistance at a given measurement frequency. Insertion loss is defined in decibels as a ratio of the output-voltage amplitude (V_D) versus the input-voltage amplitude (V_S) with a specified load impedance.

$$\text{Insertion Loss (dB)} = 20 \log \frac{|V_D|}{|V_S|}$$

At low frequencies this equation simplifies to:

$$\text{Insertion Loss (dB)} = 20 \log \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "0" Input Current (I_{INL}) — The current flowing into a digital input when a specified low-level voltage is applied to that input.

Logic "0" Input Voltage Level (V_{INL}) — The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

Logic "1" Input Voltage Level (V_{INH}) — The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

Negative Voltage Supply (V−) — The most negative voltage supply with respect to ground.

Positive Voltage Supply (V+) — The most positive voltage supply with respect to ground.

OFF Isolation ($ISO_{(OFF)}$) — The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

ON Resistance (R_{ON}) — The series ON - channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match (R_{ON} Match) — The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

$$R_{ON}\ \text{Match} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

N = # of channels in package (i.e., for MUX-08 N = 8, for MUX-16 N = 16, etc.)
R_i = Each channel's ON resistance

$$R_{AVG} = \frac{1}{N}\sum_{i=1}^{N} R_i$$

ON Resistance Variation (ΔR_{ON}) — The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON}\ (\%) = \frac{R_{ON} @ V_A = -10V - R_{ON} @ V_A = +10V}{R_{ON} @ V_A = 0V} \times 100\%$$

ON Channel Analog Leakage Current ($I_{D(ON)} + I_{S(ON)}$) Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

Output Enable Delay Time OFF ($t_{OFF(EN)}$) — Multiplexers — The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

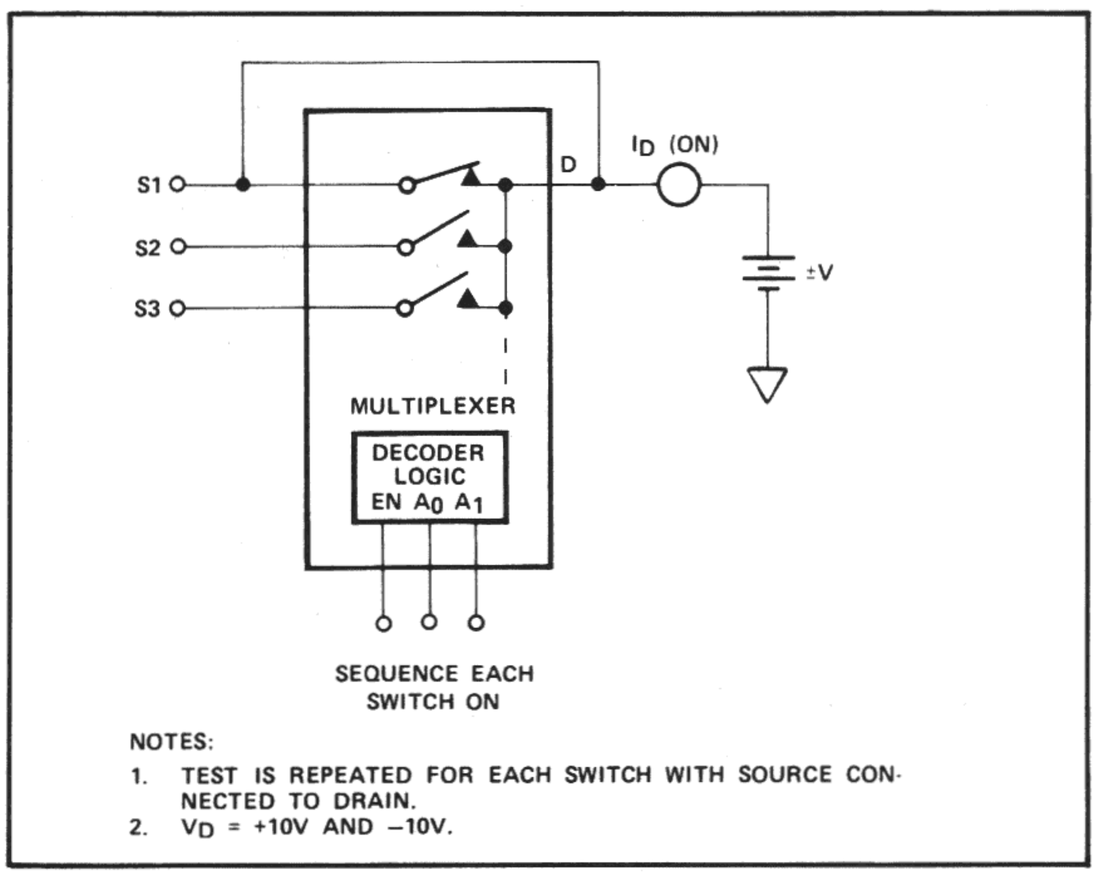
Output Enable Delay Time ON ($t_{ON(EN)}$) — Mutiplexers — The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

Output ON Switching Time (t_{ON}) — The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Output OFF Switching Time (t_{OFF}) — The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output Settling Time (t_s) — The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within specified error band.

$I_{(ON)}$ Test Condition Definitions



NOTES:
1. TEST IS REPEATED FOR EACH SWITCH WITH SOURCE CONNECTED TO DRAIN.
2. V_D = +10V AND −10V.

Power Supply Rejection (PSRR) — The ratio of the change in switch contact voltage (V_D) to the change in voltage supply (V+ or V−) that causes it.

$$+PSRR\ (dB) = 20 \log \left(\frac{\Delta V_D}{\Delta V+}\right)$$

$$-PSRR\ (dB) = 20 \log \left(\frac{\Delta V_D}{\Delta V-}\right)$$

Switching Time (t_{TRAN}) — Multiplexers — The time required to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 80% of the final value.

Total Harmonic Distortion (THD) — The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).

ANALOG SWITCHES/MULTIPLEXERS SELECTION GUIDE

One Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels V_{INL}	V_{INH}	Supply Current (mA) I+	I−
SW01	100	0.4	0.3	0	0.8	2.0	8.0	4.5
SW02	100	0.4	0.3	1	0.8	2.0	8.0	4.5

2-Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels V_{INL}	V_{INH}	Supply Current (mA) I+	I−
SSM2402	85	10000	4000	1	0.8	2.0	7.5	6.0
SSM2412	85	3500	1500	1	0.8	2.0	7.5	6.0

4-Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels V_{INL}	V_{INH}	Supply Current (mA) I+	I−
SW06	80	0.5	0.4	Note	0.8	2.0	6.0	5.0
SW201	80	0.5	0.4	0	0.8	2.0	9.0	5.0
SW202	80	0.5	0.4	1	0.8	2.0	9.0	5.0
SW7510	75	0.45	0.3	Note	0.8	2.0	9.0	5.0
SW7511	75	0.45	0.3	Note	0.8	2.0	9.0	5.0

NOTE: See individual data sheet for more details.

8-Channel MUX

Product	R_{ON} Max (Ω)	Transition Time (μs)	Logic Levels V_{INL}	Logic Levels V_{INH}	Supply Current (mA) I+	Supply Current (mA) I−
MUX08	300	2.1	0.7	2.0	12.0	3.8
MUX88	400	2.1	0.8	2.0	15.0	5.0

Dual 4-Channel MUX

Product	R_{ON} Max (Ω)	Transition Time (μs)	Logic Levels V_{INL}	Logic Levels V_{INH}	Supply Current (mA) I+	Supply Current (mA) I−
MUX24	300	2.1	0.7	2.0	12.0	3.8

16-Channel MUX

Product	R_{ON} Max (Ω)	Transition Time (μs)	Logic Levels V_{INL}	Logic Levels V_{INH}	Supply Current (mA) I+	Supply Current (mA) I−
MUX16	380	2.0	0.7	2.0	19.0	7.0

Dual 8-Channel MUX

Product	R_{ON} Max (Ω)	Transition Time (μs)	Logic Levels V_{INL}	Logic Levels V_{INH}	Supply Current (mA) I+	Supply Current (mA) I−
MUX28	380	2.0	0.7	2.0	19.0	7.0