TRI-STATE® Synchronous Counters/Latches

General Description

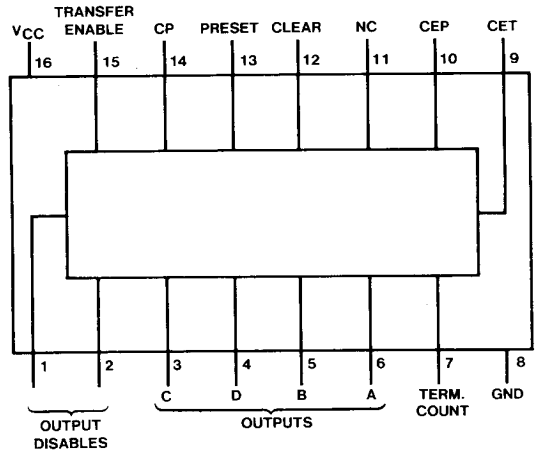
These circuits logically combine the functions of counters for frequency division, latches to store the data from the counters, and output buffer gates which provide both standard TTL outputs as well as high-impedance outputs for multiplexing of data. The counters are fully synchronous, and are made up of four edge-triggered JK flip-flops. To further facilitate operation, the Count Mode and Terminal Count outputs are also operable when the data outputs are in the high-impedance state or the latch mode.

Features

- DM7552/8552 DM75L52/85L52 — Decade counter/latch
- DM7554/8554 DM75L54/85L54 — Binary counter/latch

Type	Typical Power Dissipation	Typical Clock Frequency
52, 54	330 mW	23 MHz
L52, L54	38 mW	11 MHz

Connection Diagram



7552 (J,W) 8552 (N)
75L52 (J,W) 85L52 (N)
7554 (J,W) 8554 (N)
75L54 (J,W) 85L54 (N)

Truth Table

Inputs							Outputs				
OD1	OD2	CEP	CET	Clear	Preset	TE	A	B	C	D	TC
H	X	X	X	X	X	X	"High Impedance State"				*
X	H	X	X	X	X	X	"High Impedance State"				*
L	L	X	X	H	X	H	L	L	L	L	L
L	L	X	X	L	H	H	H	H	H	H	*
L	L	X	X	X	X	L	LATCH				*
L	L	H	H	L	L	H	COUNT				*

*Function of the count sequence.

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Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter			Conditions		DM75/85 52, 54			DM75/85 L52, L54			Units
					Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.7	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5			N/A	V
I_{OH}	High Level Output Current			DM75			−2.0			−1.0	mA
				DM85			−5.2			−1.0	
V_{OH}	High Level Output Voltage	Terminal Count	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max	I_{OH} = 0.2 mA				2.4	2.8		V
				I_{OH} = 0.4 mA	2.4	3.3					
		Others		I_{OH} = Max	2.4	3.3		2.4	2.7		
I_{OL}	Low Level Output Current			DM75			16			2.0	mA
				DM85			16			3.6	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OL} = Max	DM75		0.2	0.4		0.15	0.3	V
				DM85		0.2	0.4		0.2	0.4	
$I_{O(OFF)}$	Off State (High Impedance State) Output Current		V_{CC} = Max, V_{IH} = 2 V, V_{IL} = Max	V_O = 0.3 V						−40	μA
				V_O = 0.4 V			−40				
				V_O = 2.4 V			40			20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5 V	CET Input			2		0.02	0.2	mA
				Others			1		0.01	0.1	
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.4 V	CET Input			80		2	20	μA
				Others			40		1	10	
I_{IL}	Low Level Input Current		V_{CC} = Max, V_I = 0.4 V (Std.), V_I = 0.3 V (75L/85L)	CET Input		−2.0	−3.2		−0.24	−0.36	mA
				Others		−1.0	−1.6		−0.12	−0.18	
I_{OS}	Short Circuit Output Current		V_{CC} = Max (2)	TC Output	−20		−55	−3	−8	−15	mA
				Others	−30		−70	−3	−8	−15	
I_{CC}	Supply Current		V_{CC} = Max			66	106		7.6	13	mA

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for DM7554/8554 duration of short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From	To	Conditions			DM75 85 52, 54			DM75/85 L52, L54			Units
				Both	Std.	Low Power	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency			C_L = 50 pF	R_L = 400 Ω	R_L = 4 kΩ	15	23		6	11		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Output					34	70		115	220	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	Clock	Output					23	45		75	150	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Transfer Enable	Output					26	50		90	160	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Transfer Enable	Output					26	50		90	160	ns
t_{ZH}	Output Enable Time to High Level	Output Disable	Output					21	45		75	150	ns
t_{ZL}	Output Enable Time to Low Level	Output Disable	Output					25	50		90	150	ns
t_{HZ}	Output Disable Time from High Level	Output Disable	Output	C_L = 5 pF				3	8		8	15	ns
t_{LZ}	Output Disable Time from Low Level	Output Disable	Output					17	40		57	105	ns

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Mode of Operation

When the Transfer Enable (TE) is at a logical "1" level, the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear resets the counter to 0000.

Asynchronous Preset sets the counter to 1111. The 1111 state may be used in the 52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the 52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the 54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

(52) $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$
(54) $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counters change state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state," either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique.

Counter stages can be cascaded to provide multiple stage BCD or Binary synchronous counting by using the 52 or the 54 respectively. With a Terminal Count (TC) fan out of ten, eleven stages are able to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the TE input while the counters can continue counting. The display can be updated at any time by applying a positive pulse to the TE input.

DM7552/DM8552
DM75L52/DM85L52
DECADE COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H
**If Preset Applied Next Count	H H	H L	H L	H L	L L

**The 111 state may be used in conjunction with certain decoder/drivers (DM7446A, 7447A, 7448) for blanking leading zeroes.

DM7554/DM8554
DM75L54/DM85L54
BINARY COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

7

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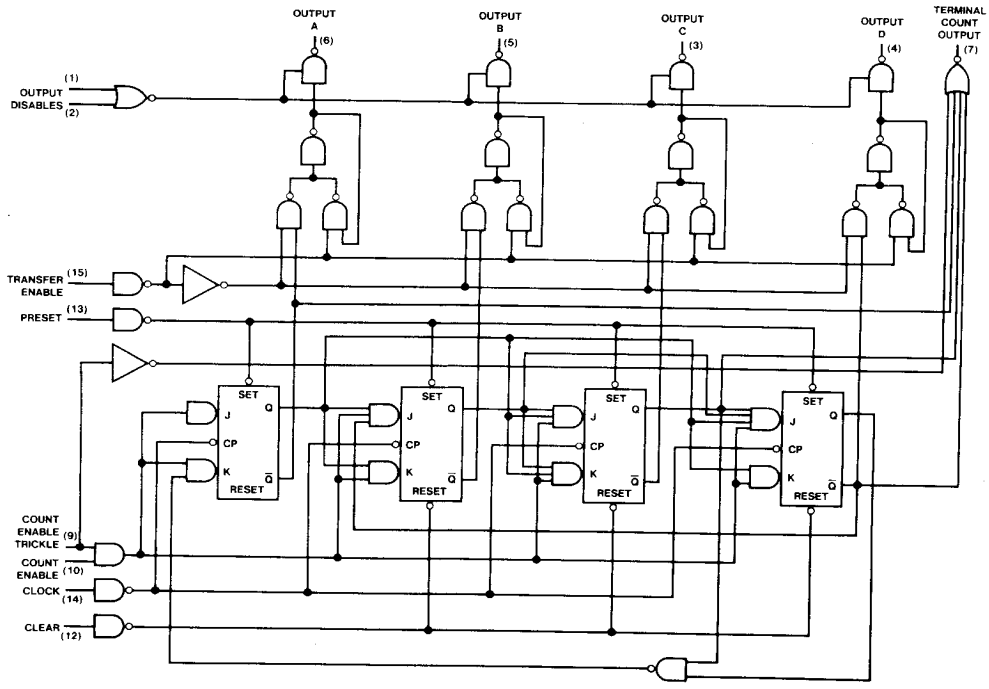
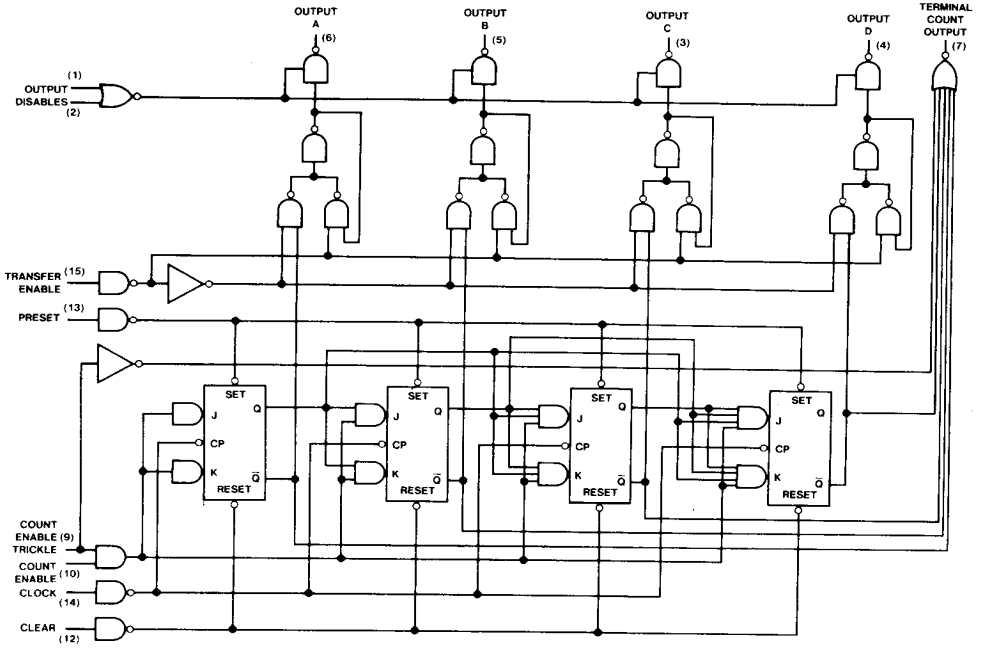
Logic Diagrams

52, L52



54, L54



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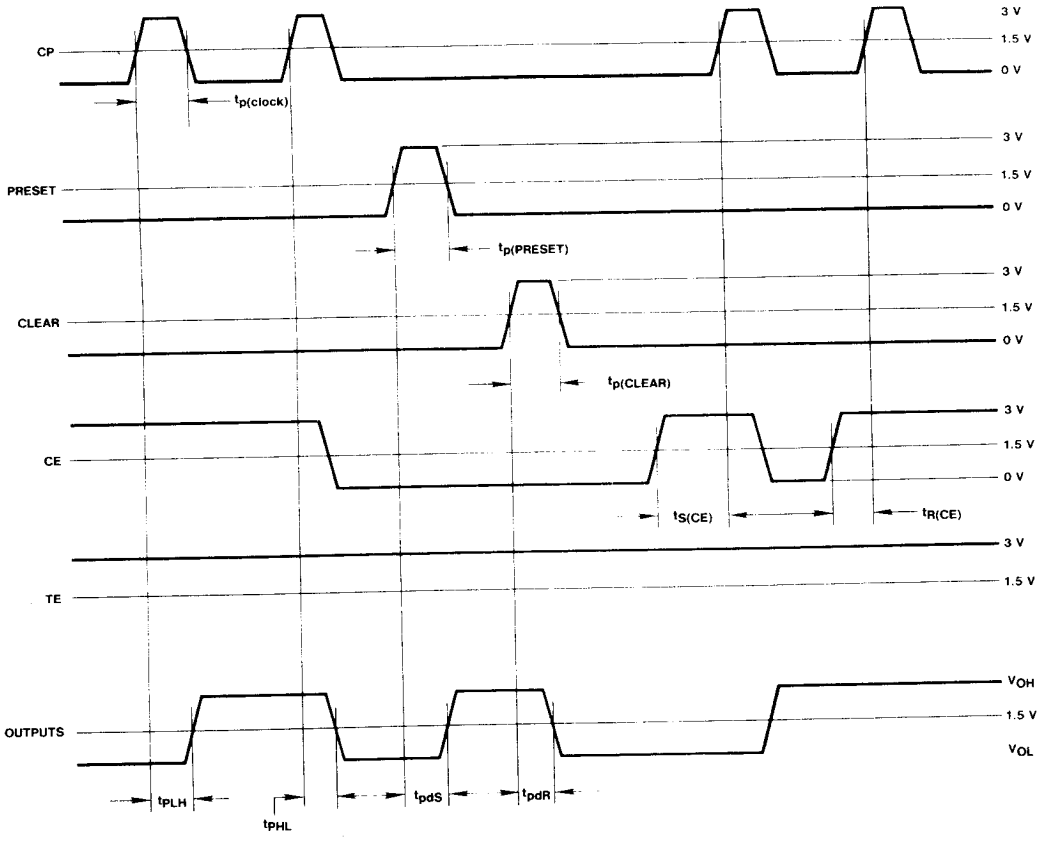
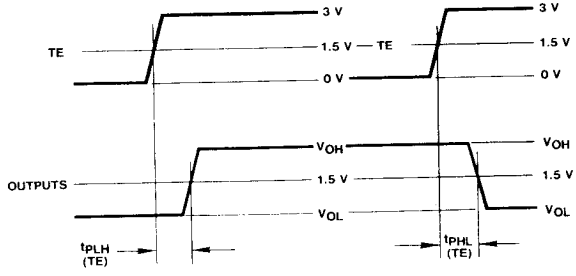
Switching Time Waveforms

52, 54





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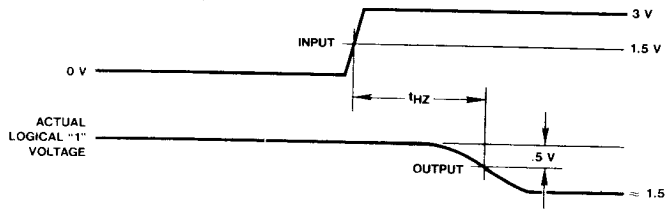
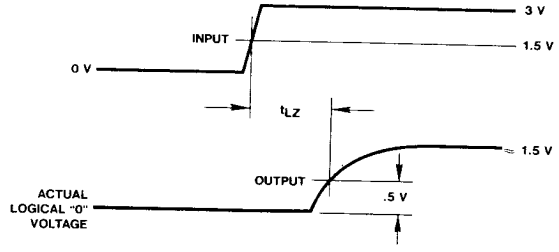
Switching Time Waveforms (Continued)

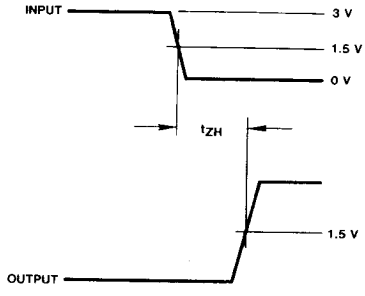
t_{HZ}



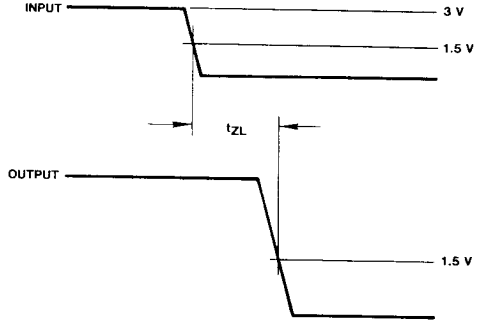
t_{LZ}



t_{ZH}



t_{ZL}



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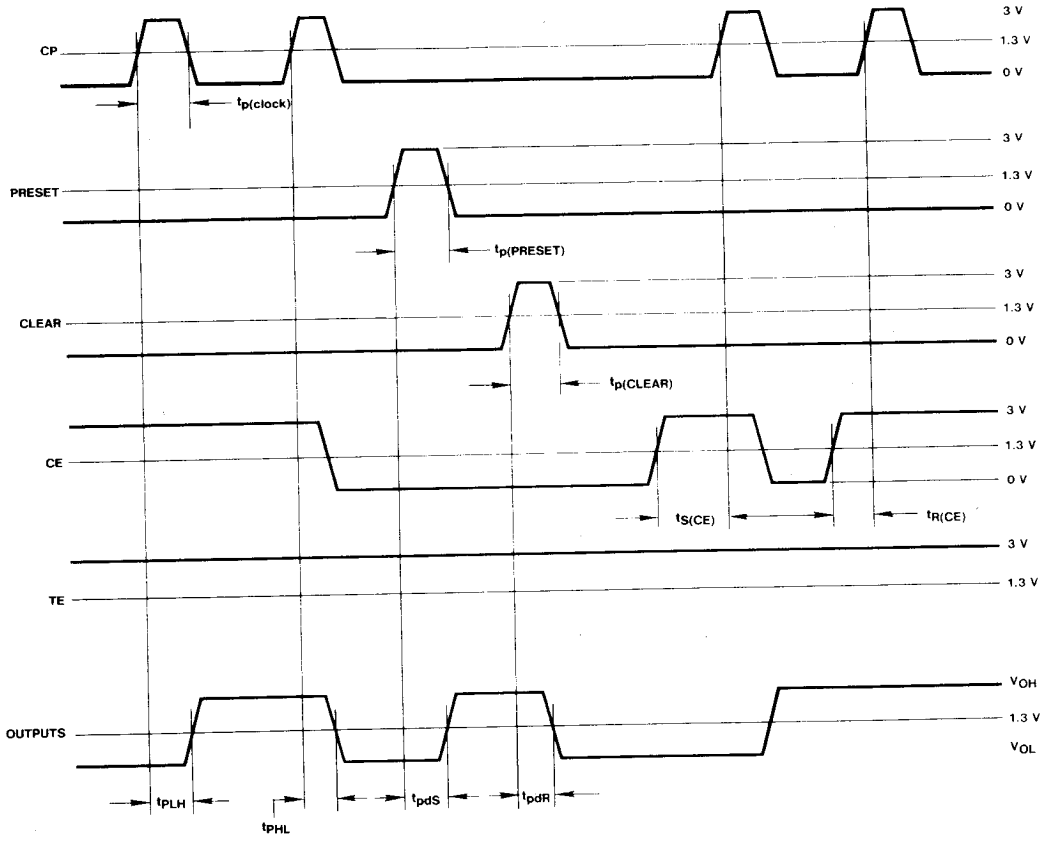
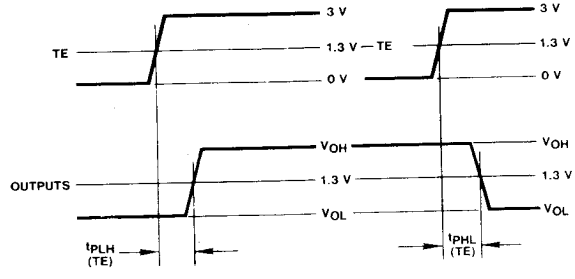
Switching Time Waveforms (Continued)

L52, L54





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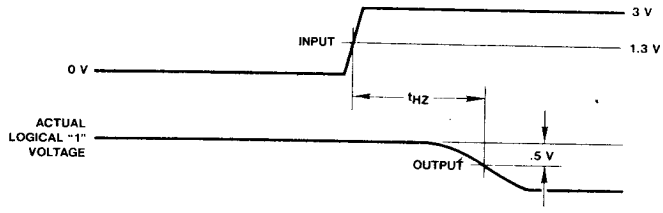
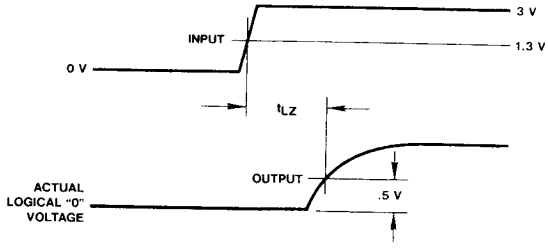
Switching Time Waveforms (Continued)

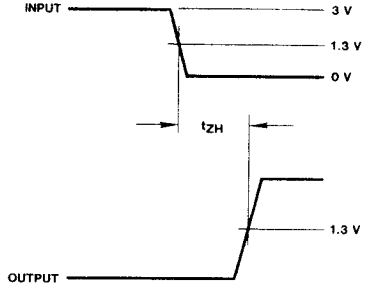
t_{HZ}



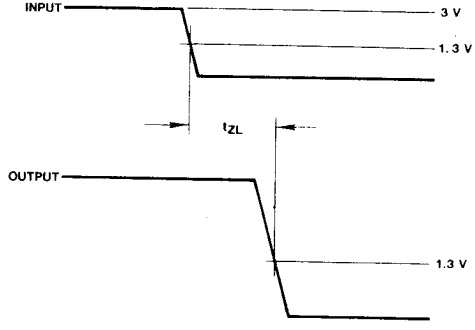
t_{LZ}



t_{ZH}



t_{ZL}



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