Drivers with Normally Open & Normally Closed Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

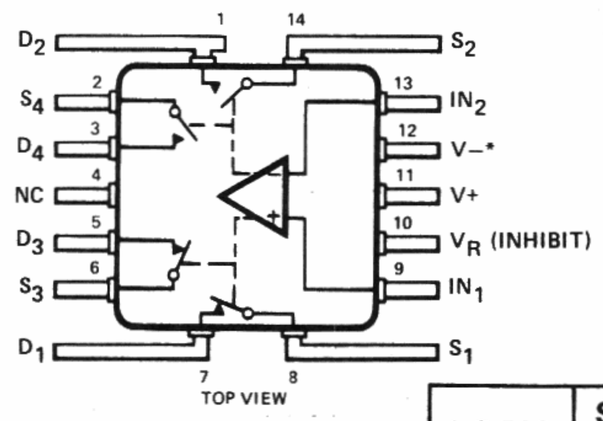
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG142 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 80 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG143 is similar to the DG142, except that it contains two FET switches instead of four. It is recommended that the DG191 and DG188 be used for new designs.

PIN CONFIGURATIONS

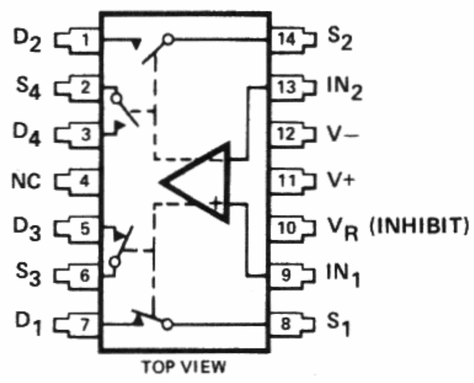
Flat Package



ORDER NUMBER:
DG142AL
SEE PACKAGE 5

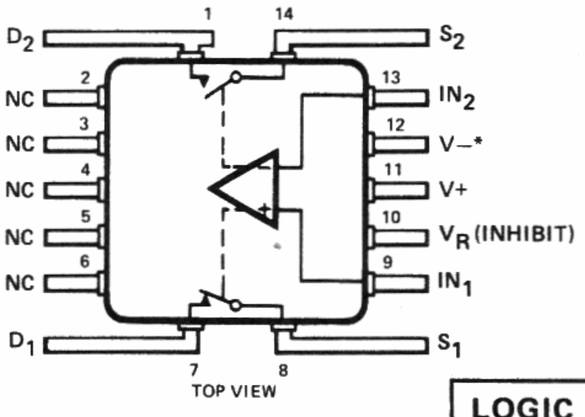
LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG142AP OR DG142BP
SEE PACKAGE 11

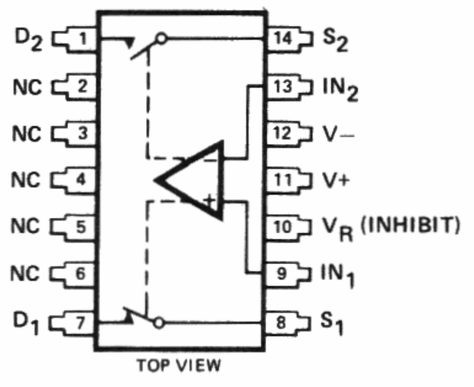
Flat Package



ORDER NUMBER:
DG143AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

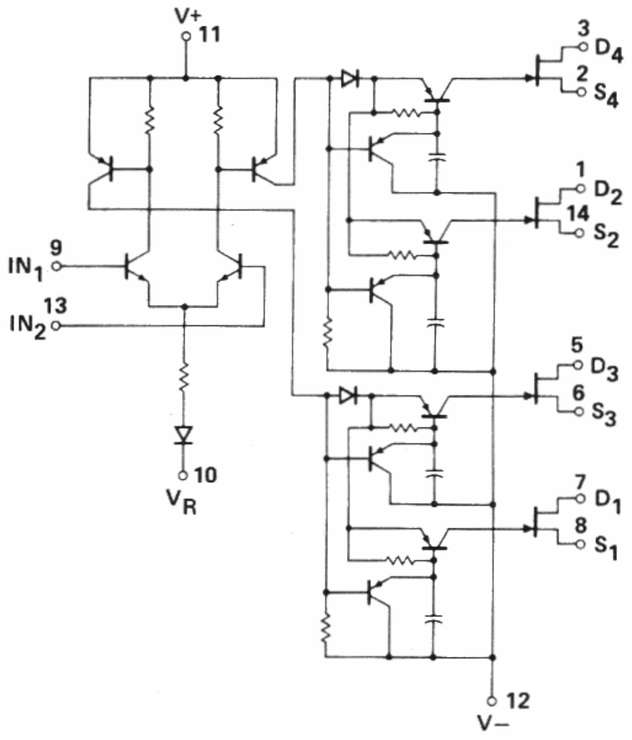


ORDER NUMBERS:
DG143AP OR DG143BP
SEE PACKAGE 11

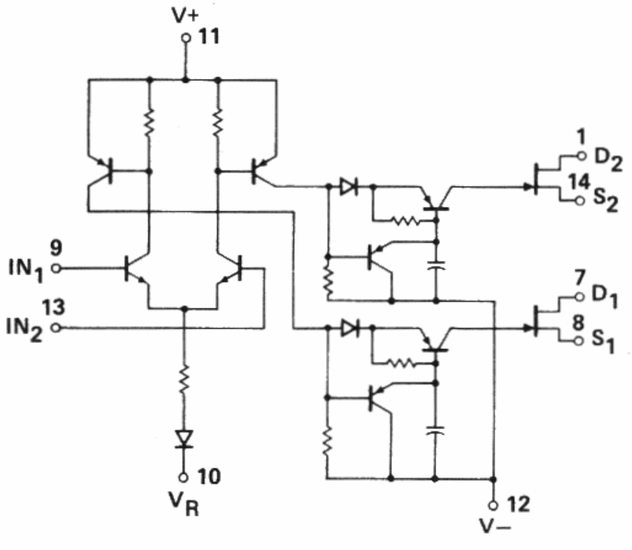
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG142



DG143

ABSOLUTE MAXIMUM RATINGS

V+ to V−, V_D or V_S	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V
Current (Any Terminal)	30 mA

Storage Temperature		−65 to 150°C
Operating Temperature	(A Suffix)	−55 to 125°C
	(B Suffix)	−20 to 85°C
Power Dissipation*		
Flat Package**		750 mW
14 Pin DIP***		825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

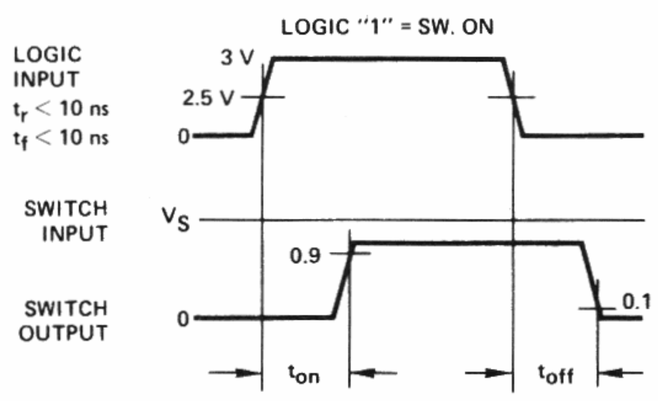
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	80	80	150				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							100	100	150		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15		$C_{S(off)}$	Source OFF Capacitance		**2.4 Typ			**2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		**2.4 Typ			**2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		**2.8 Typ			**2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

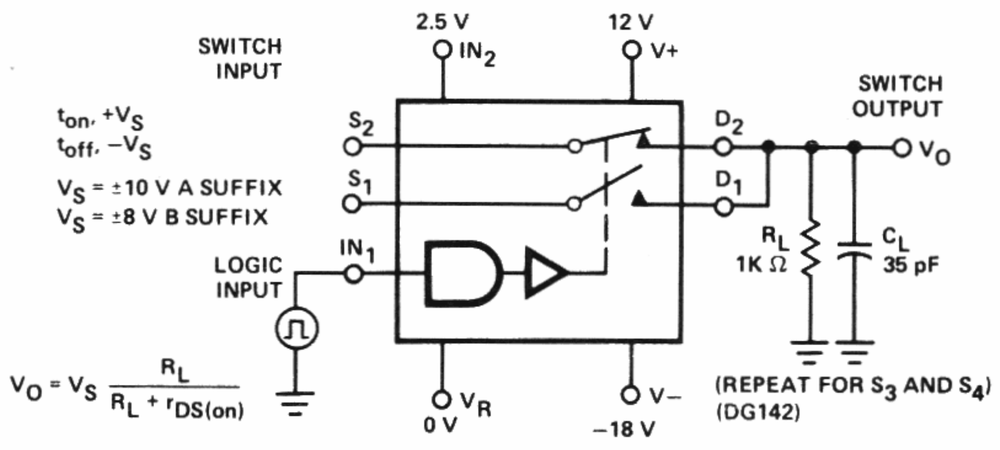
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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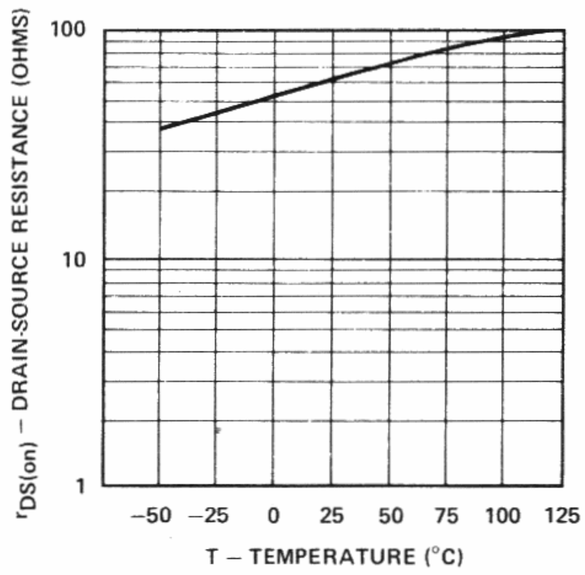
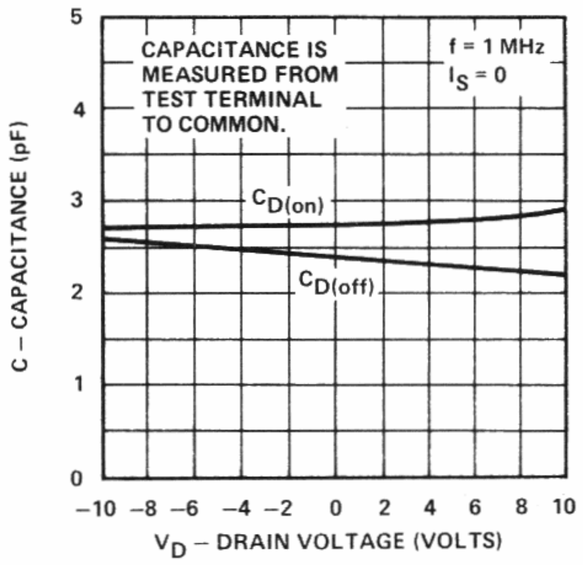
TYPICAL CHARACTERISTICS

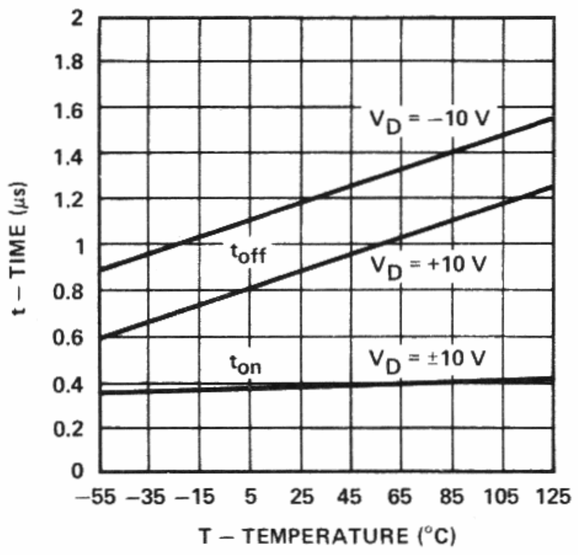
$r_{DS(on)}$ vs Temperature



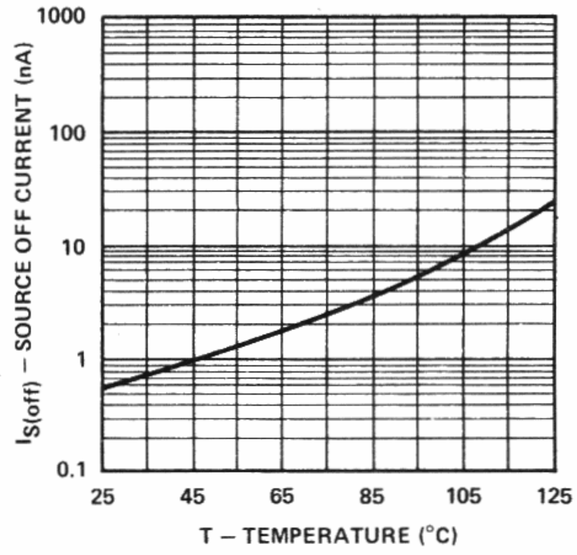
Capacitance vs V_D



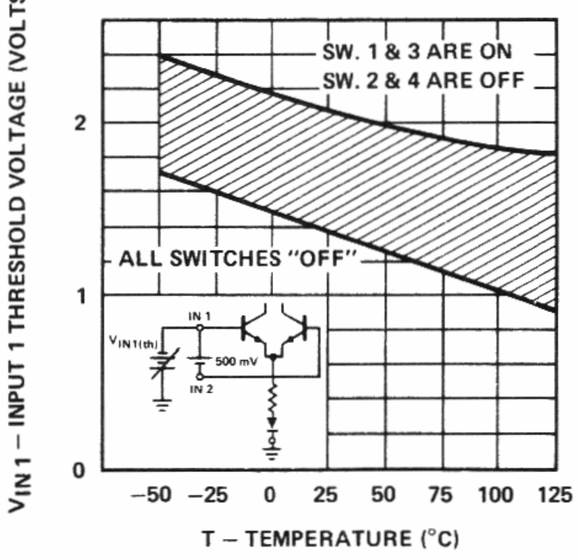
Switching Time vs V_D and Temperature



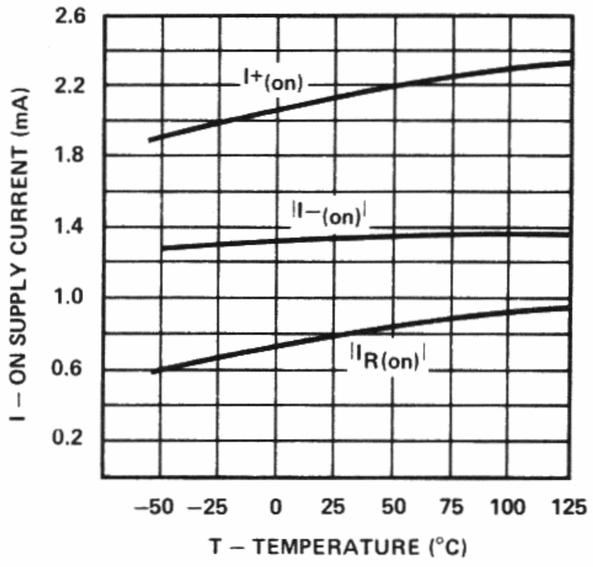
$I_{S(off)}$ vs Temperature



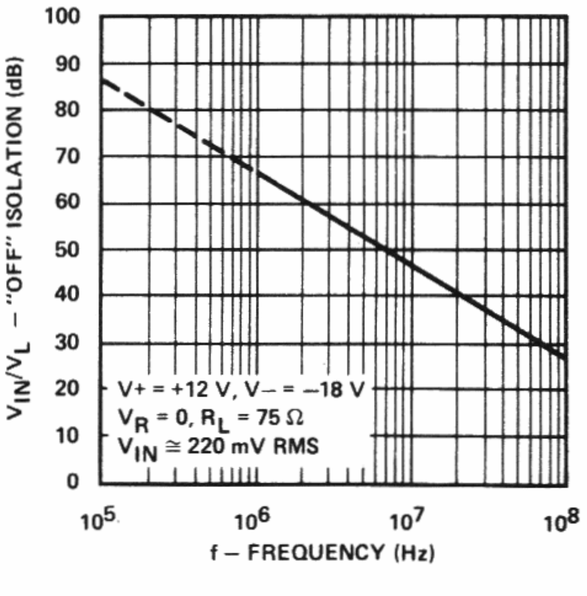
$V_{IN(th)}$ vs Temperature



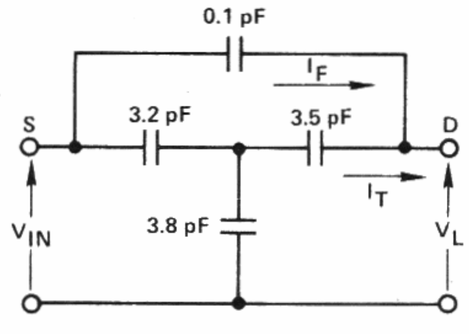
Supply Current vs Temperature



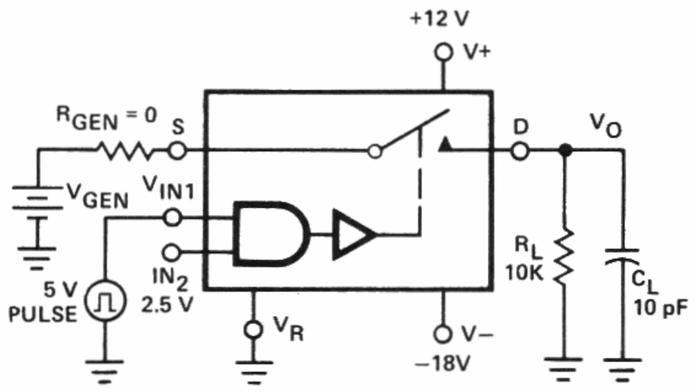
"OFF" Isolation vs R_L and Frequency



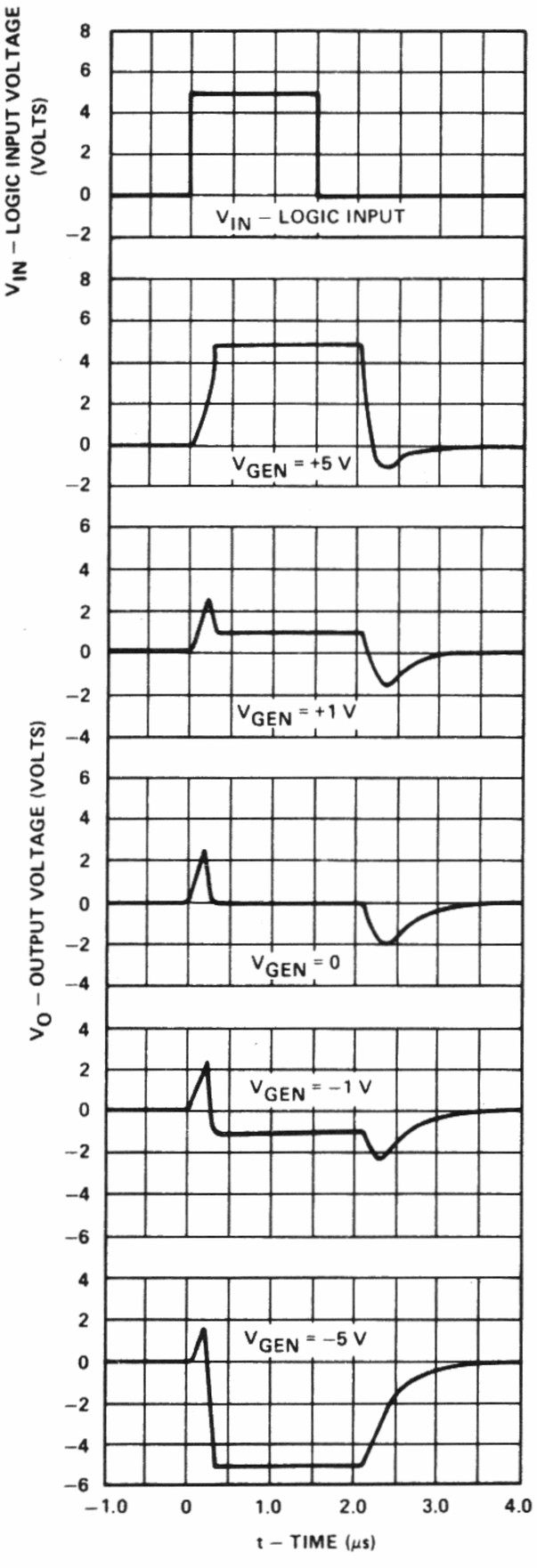
Equivalent "OFF" Circuit

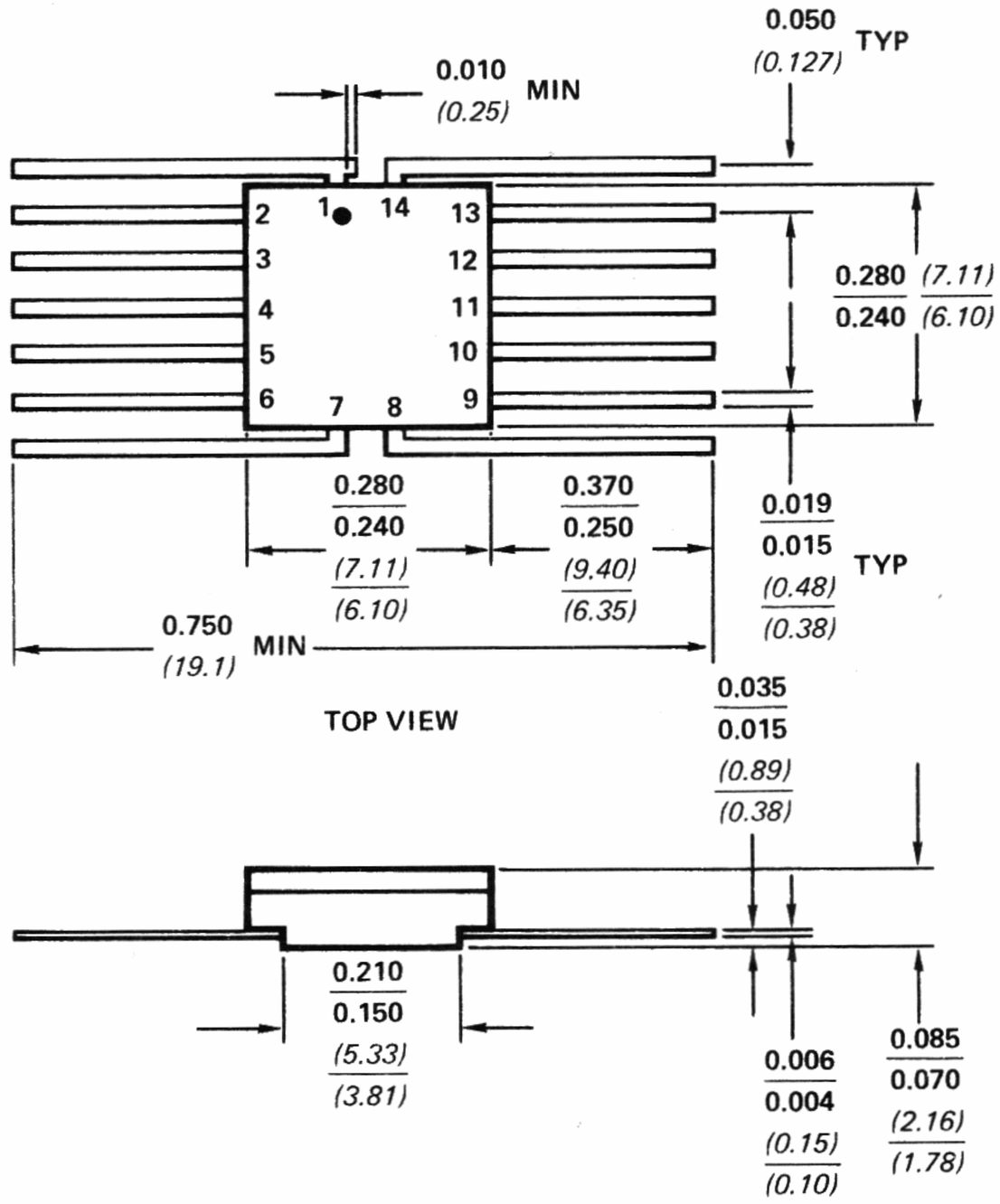


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



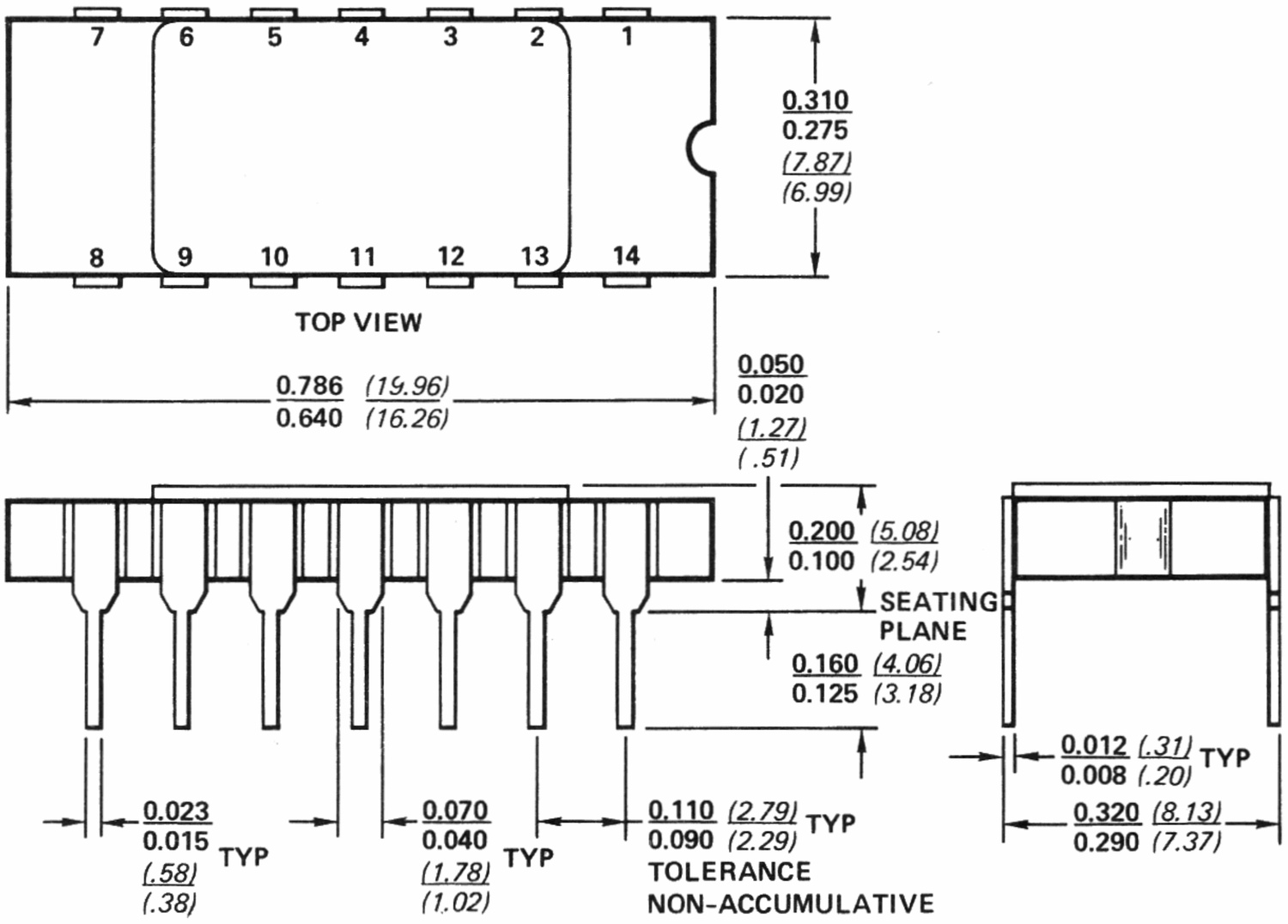


PACKAGE 5
14 LEAD FLATPAC (L)
(BOTTOM BRAZE)

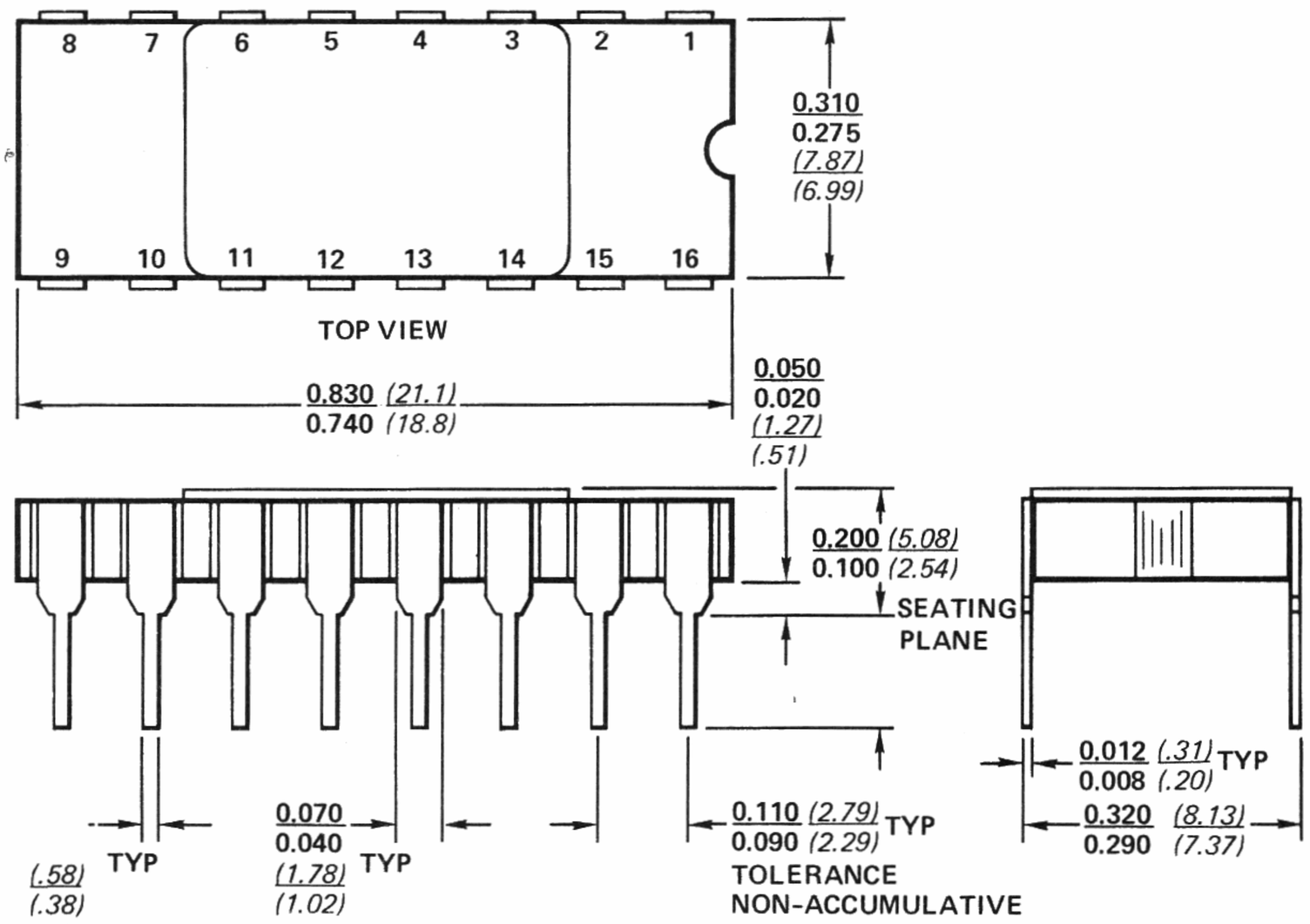
PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 11
14 LEAD DUAL IN LINE PACKAGE **(P)**
(SIDE BRAZE)



PACKAGE 12
16 LEAD DUAL IN LINE PACKAGE **(P)**
(SIDE BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)