

Silicon NPN Power Transistors

BDV65/65A/65B/65C

DESCRIPTION

- With TO-3PN package
- Complement to type BDV64/64A/64B/64C
- DARLINGTON
- High DC current gain

APPLICATIONS

- For use in general purpose amplifier applications.

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

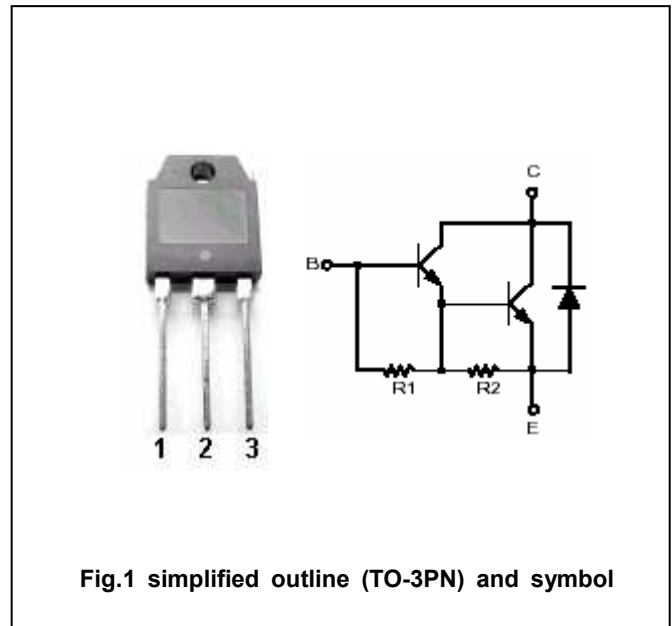


Fig.1 simplified outline (TO-3PN) and symbol

Absolute maximum ratings($T_c=25^\circ$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	BDV65	60	V
		BDV65A	80	
		BDV65B	100	
		BDV65C	120	
V_{CEO}	Collector-emitter voltage	BDV65	60	V
		BDV65A	80	
		BDV65B	100	
		BDV65C	120	
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		12	A
I_{CM}	Collector current-peak		15	A
I_B	Base current		0.5	A
P_C	Collector power dissipation	$T_c=25^\circ$	125	W
		$T_a=25^\circ$	3.5	
T_j	Junction temperature		150	$^\circ$
T_{stg}	Storage temperature		-65~150	$^\circ$

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	
V _{(BR)CEO}	Collector-emitter breakdown voltage	BDV65	60			V	
		BDV65A	80				
		BDV65B	100				
		BDV65C	120				
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A, I _B =20mA			2.0	V	
V _{BE}	Base-emitter on voltage	I _C =5A; V _{CE} =4V			2.5	V	
I _{CBO}	Collector cut-off current	BDV65	V _{CB} =60V, I _E =0 V _{CB} =30V, I _E =0; T _C =150 °C			0.4 2.0	mA
		BDV65A	V _{CB} =80V, I _E =0 V _{CB} =40V, I _E =0; T _C =150 °C			0.4 2.0	
		BDV65B	V _{CB} =100V, I _E =0 V _{CB} =50V, I _E =0; T _C =150 °C			0.4 2.0	
		BDV65C	V _{CB} =120V, I _E =0 V _{CB} =60V, I _E =0; T _C =150 °C			0.4 2.0	
I _{CEO}	Collector cut-off current	BDV65	V _{CE} =30V, I _B =0			2	mA
		BDV65A	V _{CE} =40V, I _B =0				
		BDV65B	V _{CE} =50V, I _B =0				
		BDV65C	V _{CE} =60V, I _B =0				
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			5	mA	
h _{FE}	DC current gain	I _C =5A; V _{CE} =4V	1000				
V _{EC}	Diode forward voltage	I _E =10A			3.5	V	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
R _{th j-c}	Thermal resistance junction to case	1.0	°C/W

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PACKAGE OUTLINE

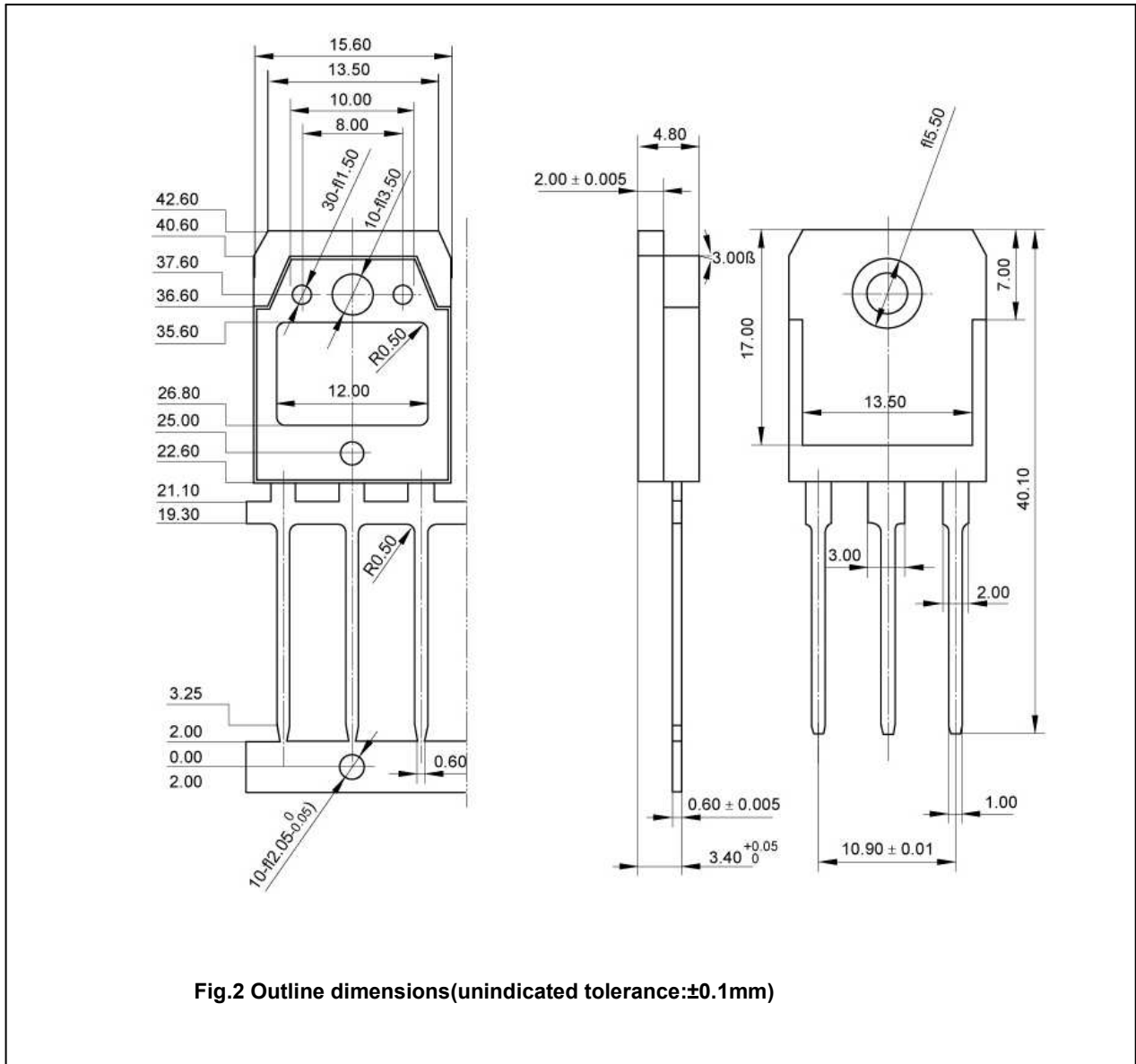


Fig.2 Outline dimensions(unindicated tolerance:±0.1mm)

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.