

# EFCIS

THOMSON-EFCIS MOS Integrated Circuits

mosmos mosmos mosmos

## HEX THREE-STATE BUFFER INVERTERS

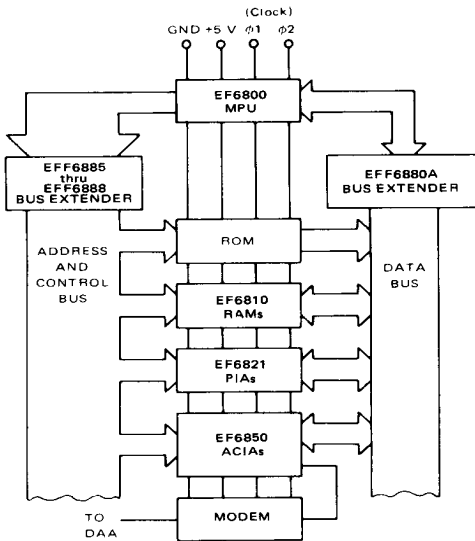
This series of devices combines three features usually found desirable in bus-oriented systems : 1) High impedance logic inputs insure that these devices do not seriously load the bus ; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus ; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting EFF6885 and inverting EFF6886 provide a two-input Enable which controls all six buffers, while the non-inverting EFF6887 and inverting EFF6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the EF6800 or similar microprocessor application.

- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or EF6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus
- Pin for pin compatible with MC8T95, MC8T96, MC8T97, MC8T98.

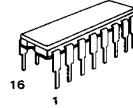
## MICROPROCESSOR BUS EXTENDER APPLICATION



EF6885  
EF6886  
EF6887  
EF6888

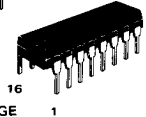
## HEX THREE-STATE BUFFER/INVERTERS

CASE CB-79

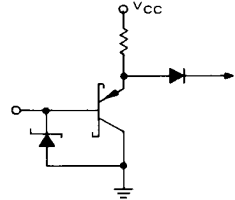


P SUFFIX  
PLASTIC PACKAGE

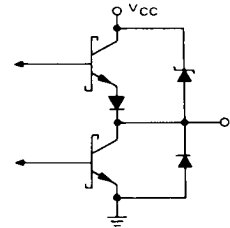
C SUFFIX  
CERAMIC PACKAGE



## INPUT EQUIVALENT CIRCUIT



## OUTPUT EQUIVALENT CIRCUIT



## ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

DEVICE	PACKAGE
EFF6885C	Ceramic DIP
EFF6886C	Ceramic DIP
EFF6887C	Ceramic DIP
EFF6888C	Ceramic DIP
EFF6885P	Plastic DIP
EFF6886P	Plastic DIP
EFF6887P	Plastic DIP
EFF6888P	Plastic DIP

DS9457-A

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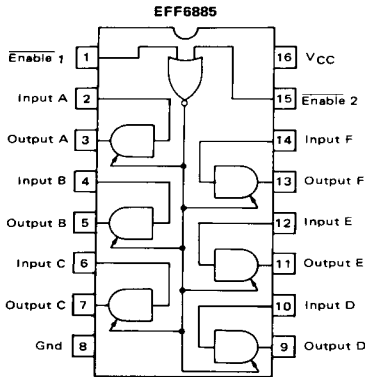
45, av. de l'Europe  
78140 VELIZY

**EFCIS**  
FRANCE

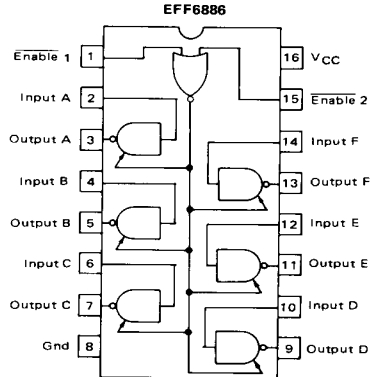
Tel.:(3) 946 97 19  
Telex : 698866F

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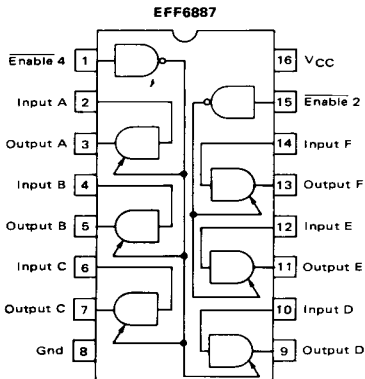
PIN CONNECTIONS AND TRUTH TABLES



Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
L	L	X	Z
H	L	X	Z
H	H	X	Z

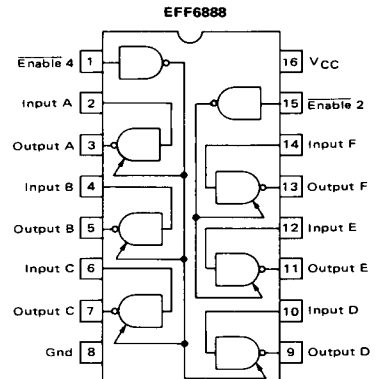


Enable 2	Enable 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
L	L	X	Z
H	L	X	Z
H	H	X	Z



Enable	Input	Output
L	L	L
L	H	H
L	X	Z
H	X	Z

L = Low Logic State  
 H = High Logic State  
 Z = Third (High Impedance) State  
 X = Irrelevant



Enable	Input	Output
L	L	H
L	H	L
L	X	Z
H	X	Z

MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	8.0	Vdc
Input Voltage	V <sub>I</sub>	5.5	Vdc
Operating Ambient Temperature Range	T <sub>A</sub>	0 to +75	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>		°C
Plastic Package		150	
Ceramic Package		175	

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted,  $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$  and  $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ )

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State ( $V_{CC} = 4.75\text{ V}$ , $T_A = 25^{\circ}\text{C}$ )	$V_{IH}$	2.0	–	–	V
Input Voltage – Low Logic State ( $V_{CC} = 4.75\text{ V}$ , $T_A = 25^{\circ}\text{C}$ )	$V_{IL}$	–	–	0.8	V
Input Current – High Logic State ( $V_{CC} = 5.25\text{ V}$ , $V_{IH} = 2.4\text{ V}$ )	$I_{IH}$	–	–	40	$\mu\text{A}$
Input Current – Low Logic State ( $V_{CC} = 5.25\text{ V}$ , $V_{IL} = 0.5\text{ V}$ , $V_{IL(E)} = 0.5\text{ V}$ )	$I_{IL}$	–	–	-400	$\mu\text{A}$
Input Current – High Impedance State ( $V_{CC} = 5.25\text{ V}$ , $V_{IL(I)} = 0.5\text{ V}$ , $V_{IH(E)} = 2.0\text{ V}$ )	$I_{IH(E)}$	–	–	-40	$\mu\text{A}$
Output Voltage – High Logic State ( $V_{CC} = 4.75\text{ V}$ , $I_{OH} = -5.2\text{ mA}$ )	$V_{OH}$	2.4	–	–	V
Output Voltage – Low Logic State ( $I_{OL} = 48\text{ mA}$ )	$V_{OL}$	–	–	0.5	V
Output Current – High Impedance State ( $V_{CC} = 5.25\text{ V}$ , $V_{OH} = 2.4\text{ V}$ ) ( $V_{CC} = 5.25\text{ V}$ , $V_{OL} = 0.5\text{ V}$ )	$I_{OZ}$	–	–	40 -40	$\mu\text{A}$
Output Short-Circuit Current ( $V_{CC} = 5.25\text{ V}$ , $V_O = 0$ ) (only one output can be shorted at a time)	$I_{OS}$	-40	-80	-115	mA
Power Supply Current ( $V_{CC} = 5.25\text{ V}$ )	$I_{CC}$	–	65 59	98 89	mA
Input Clamp Voltage ( $V_{CC} = 4.75\text{ V}$ , $I_{IC} = -12\text{ mA}$ )	$V_{IC}$	–	–	-1.5	V
Output $V_{CC}$ Clamp Voltage ( $V_{CC} = 0$ , $I_{OC} = 12\text{ mA}$ )	$V_{OC}$	–	–	1.5	V
Output Gnd Clamp Voltage ( $V_{CC} = 0$ , $I_{OC} = -12\text{ mA}$ )	$V_{OC}$	–	–	-1.5	V
Input Voltage ( $I_I = 1.0\text{ mA}$ )	$V_I$	5.5	–	–	V

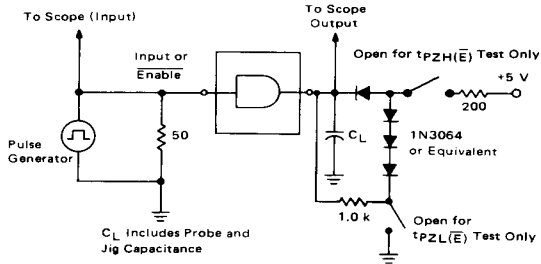
**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$  unless otherwise noted.)

Characteristic	Symbol	EFF6885/87			EFF6886/88			Unit
		Min	Typ	Max	Min	Typ	Min	
Propagation Delay Time – High to Low State ( $C_L = 50\text{ pF}$ ) ( $C_L = 250\text{ pF}$ ) ( $C_L = 375\text{ pF}$ ) ( $C_L = 500\text{ pF}$ )	$t_{PHL}$	3.0 – – –	– 16 20 23	12 – – –	4.0 – – –	– 15 18 22	11 – – –	ns
Propagation Delay Time – Low to High State ( $C_L = 50\text{ pF}$ ) ( $C_L = 250\text{ pF}$ ) ( $C_L = 375\text{ pF}$ ) ( $C_L = 500\text{ pF}$ )	$t_{PLH}$	3.0 – – –	– 25 33 42	13 – – –	3.0 – – –	– 22 28 35	10 – – –	ns
Transition Time – High to Low State ( $C_L = 250\text{ pF}$ ) ( $C_L = 375\text{ pF}$ ) ( $C_L = 500\text{ pF}$ )	$t_{THL}$	– – –	10 11 14	– – –	– – –	10 13 15	– – –	ns
Transition Time – Low to High State ( $C_L = 250\text{ pF}$ ) ( $C_L = 375\text{ pF}$ ) ( $C_L = 500\text{ pF}$ )	$t_{TLH}$	– – –	32 42 60	– – –	– – –	28 38 53	– – –	ns

**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	EFF6885/87			EFF6886/88			Unit
		Min	Typ	Max	Min	Typ	Min	
Propagation Delay Time — High State to Third State ( $C_L = 5.0 \text{ pF}$ )	$t_{PHZ}(\bar{E})$	3.0	—	10	3.0	—	10	ns
Propagation Delay Time — Low State to Third State ( $C_L = 5.0 \text{ pF}$ )	$t_{PLZ}(\bar{E})$	3.0	—	12	5.0	—	16	ns
Propagation Delay Time — Third State to High State ( $C_L = 50 \text{ pF}$ )	$t_{PZH}(\bar{E})$	8.0	—	25	7.0	—	22	ns
Propagation Delay Time — Third State to Low State ( $C_L = 50 \text{ pF}$ )	$t_{PZL}(\bar{E})$	12	—	25	11	—	24	ns

**FIGURE 1 — TEST CIRCUIT FOR SWITCHING CHARACTERISTICS**



**FIGURE 2 — WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT**

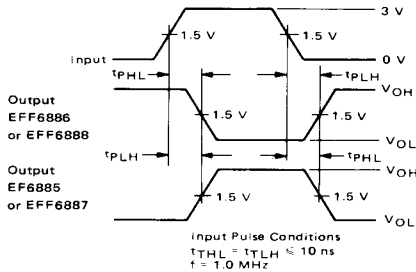
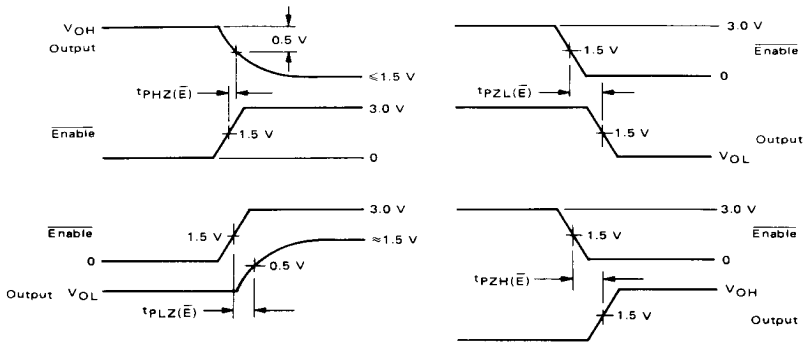
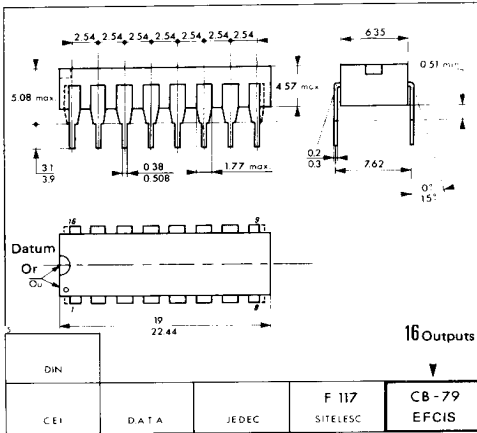


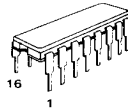
FIGURE 3 - WAVEFORMS FOR PROPAGATION DELAY TIMES - ENABLE TO OUTPUT



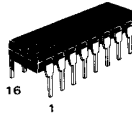
H = High-Logic State, L = Low-Logic State, Z = High Impedance State



CASE CB-79



C SUFFIX  
CERAMIC PACKAGE



P SUFFIX  
PLASTIC PACKAGE

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$PD(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

Where:  $PD(T_A)$  = Power Dissipation allowable at a given operating ambient temperature. This must be greater than

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$  = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section  
 $T_A$  = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$  = Typical Thermal Resistance Junction to Ambient

These specifications are subject to change without notice.  
 Please inquire with our sales offices about the availability of the different packages.