DG200

Dual Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e. Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **TTL Compatible Switching Systems**
- **High Frequency Signal Switching, such as Video Signals**

BENEFITS

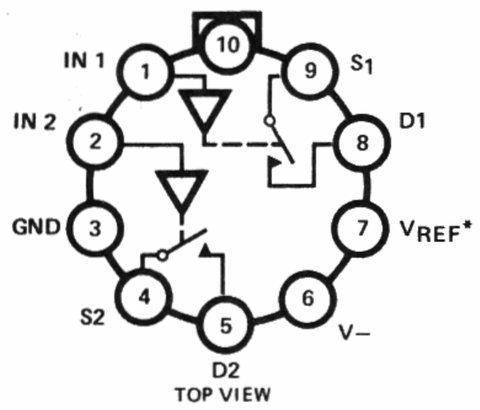
- **Environmentally Rugged**
  - Latch-proof CMOS
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 10 pA Typical Leakage From Source or Drain
  - Low Charge Coupling

DESCRIPTION

The DG200 is a 2-channel, single-pole, single-throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.

PIN CONFIGURATIONS

Metal Can Package



TOP VIEW

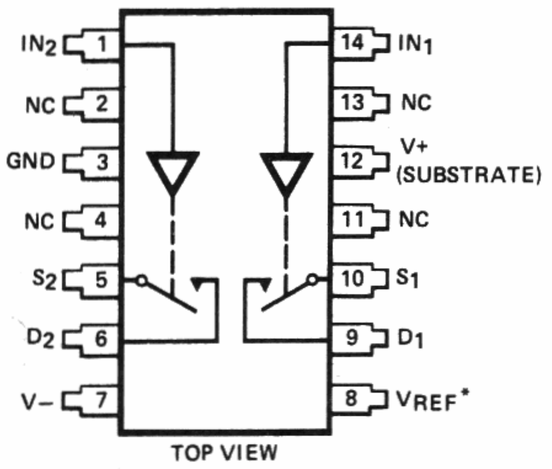
ORDER NUMBERS:
DG200AA OR DG200BA
SEE PACKAGE 2

LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG200AP OR DG200BP
SEE PACKAGE 11

DG200CJ
SEE PACKAGE 7

Dual-In-Line Package

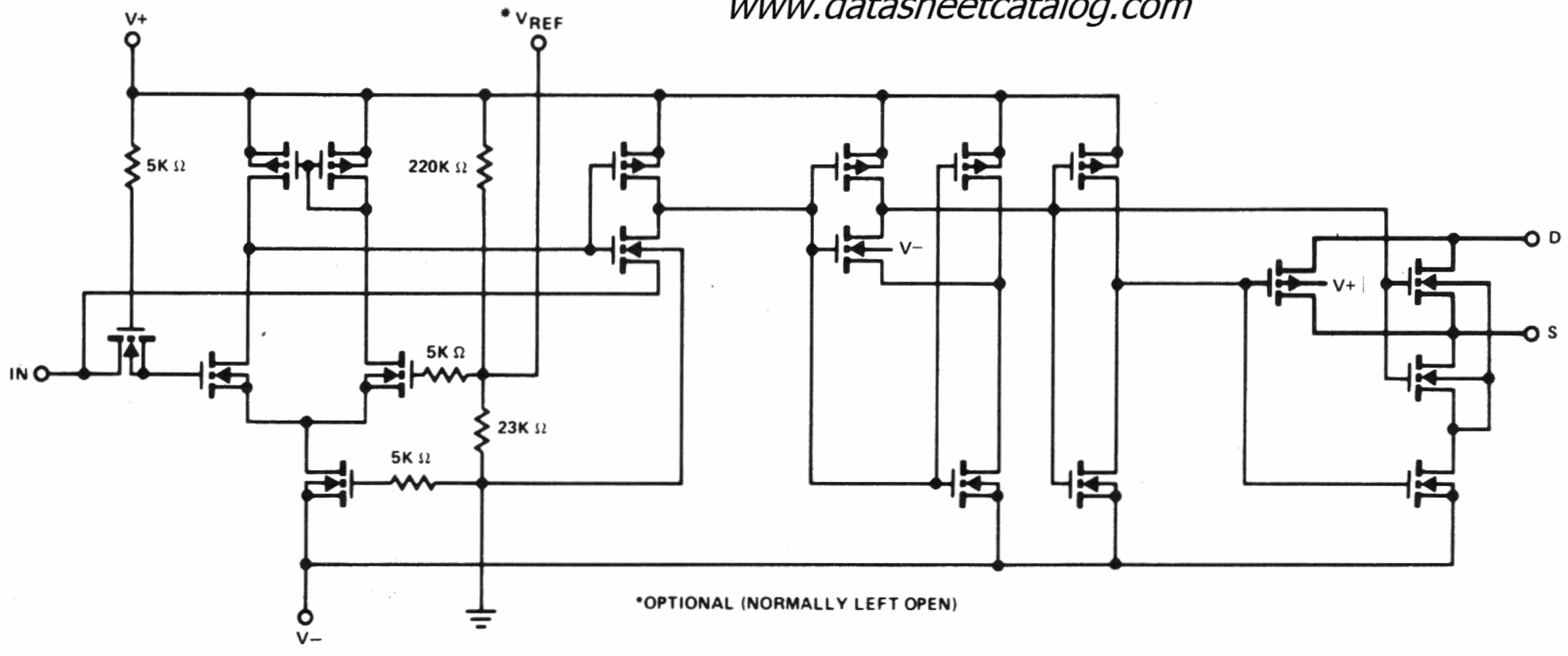


TOP VIEW

*Optional (Normally Left Open)

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (Typical Channel)



*OPTIONAL (NORMALLY LEFT OPEN)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground	−0.3 V, V+
V_S or V_D to V+	0, −32 V
V_S or V_D to V−	0, 32 V
V+ to Ground	16 V
V− to Ground	−16 V
Current, Any Terminal Except S or D	30 mA
Current, S or D	20 mA
Current, S or D Pulsed (1 msec, 10% Duty Cycle Max)	100 mA
Operating Temp. (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Storage Temp. (A & B Suffix)	−65 to 150°C
(C Suffix)	−65 to +125°C
Power Dissipation (Package)*	
Metal Can**	450 mW
14 Pin DIP***	825 mW
14 Pin Plastic DIP****	470 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

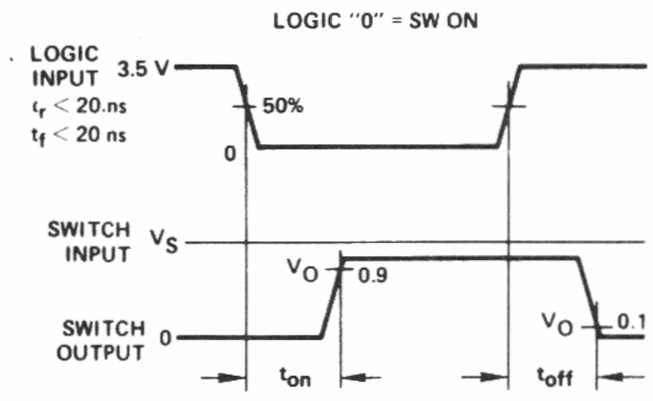
		CHARACTERISTIC		TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_{REF} = Open***	
1	SWITCH	V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = −10 V	V_{IN} = 0.8 V, I_S = −1 mA
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	+0.01		2	100		5	100	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	−0.02		−2	−100		−5	−100	nA	V_S = −14V, V_D = 14 V	V_{IN} = 2.4 V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	+0.01		2	100		5	100	nA	V_D = 14 V, V_S = −14 V	V_{IN} = 2.4 V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	−0.02		−2	−100		−5	−100	nA	V_D = −14 V, V_S = 14 V	V_{IN} = 2.4 V
8	SWITCH	$I_{D(on)}$*	Channel ON Leakage Current	+0.1		2	200		−5	200	nA	V_D = V_S = 14 V	V_{IN} = 0.8 V
9	SWITCH	$I_{D(on)}$*	Channel ON Leakage Current	−0.1		−2	−200		−5	−200	nA	V_D = V_S = −14 V	V_{IN} = 0.8 V
10	INPUT	I_{INH}	Input Current Input Voltage High	0.0009		−1	−10		−1	−10	μA	V_{IN} = 2.4 V	
11	INPUT	I_{INH}	Input Current Input Voltage High	0.005		1	10		1	10	μA	V_{IN} = 15 V	
12	INPUT	$I_{IN(peak)}$	Peak Input Current Required for Transition	−150							μA	See Curve I_{IN} vs V_{IN}	
13	INPUT	I_{INL}	Input Current, Input Voltage Low	−.0015		−1	−10		−1	−10	μA	V_{IN} = 0 V	
14	DYNAMIC	t_{on}	Turn-ON Time	440		1000			1000		ns	See Switching Time Test Circuit	
15	DYNAMIC	t_{off}	Turn-OFF Time	370		500			500		ns	See Switching Time Test Circuit	
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	9.0							pF	V_S = 0, V_{IN} = 5 V	
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	9.0							pF	V_D = 0, V_{IN} = 5 V	f = 140 kHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	25							pF	V_D = V_S = 0, V_{IN} = 0	
19	DYNAMIC	OFF Isolation		72							dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 7 VRMS, f = 500 kHz	
20	SUP	I+	Positive Supply Current	+2.3		4			4		mA	Both Channels "ON," V_{IN} = 0	
21	SUP	I−	Negative Supply Current	−2.3		−4			−4		mA	Both Channels "ON," V_{IN} = 0	
22	SUP	I+ Standby	Positive Supply Current	+0.7		2			2		mA	Both Channels "OFF," V_{IN} = 5 V	
23	SUP	I− Standby	Negative Supply Current	−0.6		−2			−2		mA	Both Channels "OFF," V_{IN} = 5 V	

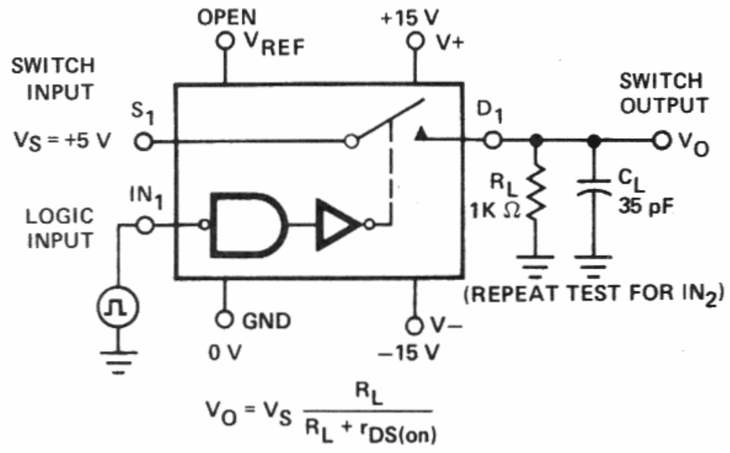
ICXE

NOTES:
†Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
*$I_{D(on)}$ is leakage from driver into "ON" switch.
**"OFF" isolation $\triangleq$ 20 log V_S/V_D, V_S = input to OFF switch, V_D = output
***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = −V− = 10 V, 1.4 V may be applied to V_{REF} terminal. The V_{REF} terminal has $R_{IN} \cong$ 21K Ω. See Applications Section.

SWITCHING TIME TEST CIRCUIT

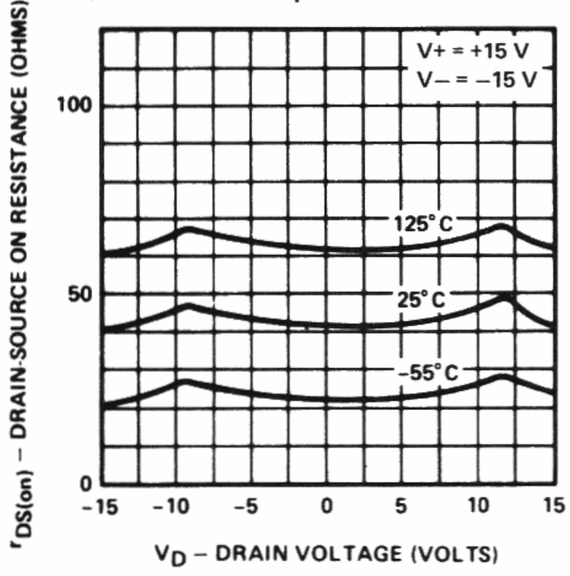
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



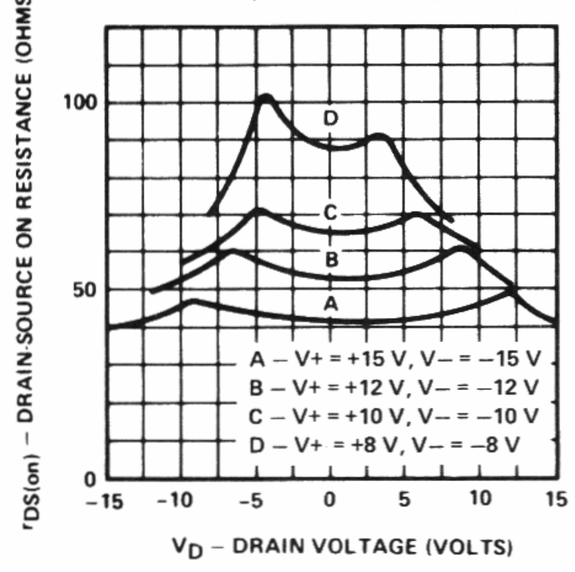


TYPICAL CHARACTERISTICS

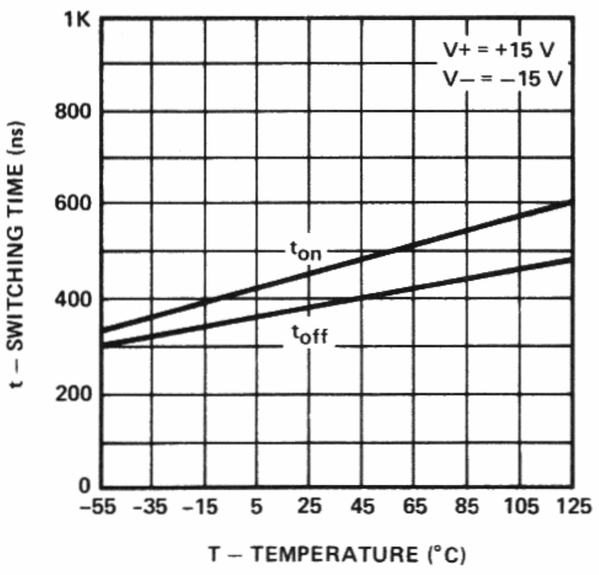
$r_{DS(on)}$ vs V_D and Temperature



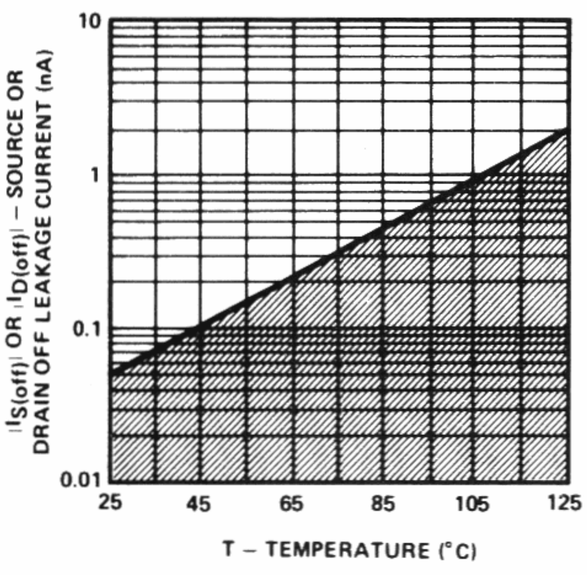
$r_{DS(on)}$ vs V_D and Power Supply Voltage



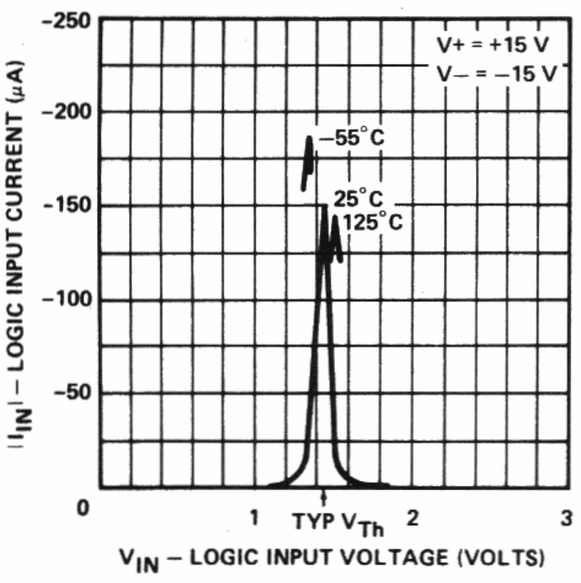
Switching Time vs Temperature



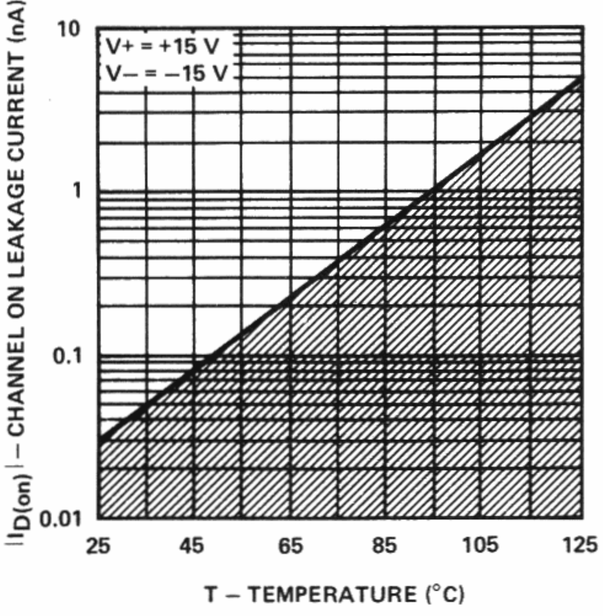
$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



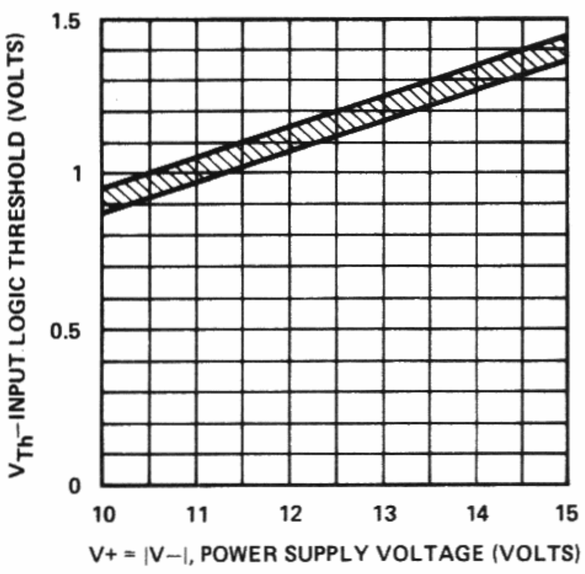
I_{IN} vs V_{IN}



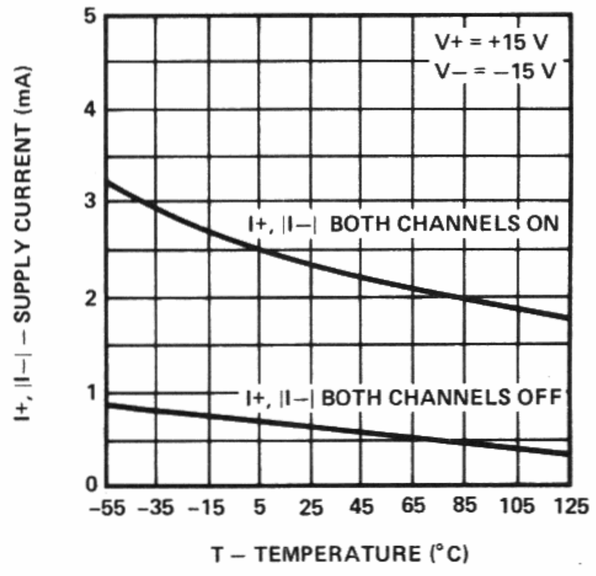
$I_{D(on)}$ vs Temperature*



V_{Th} (Input Logic Threshold) vs Power Supply Voltage

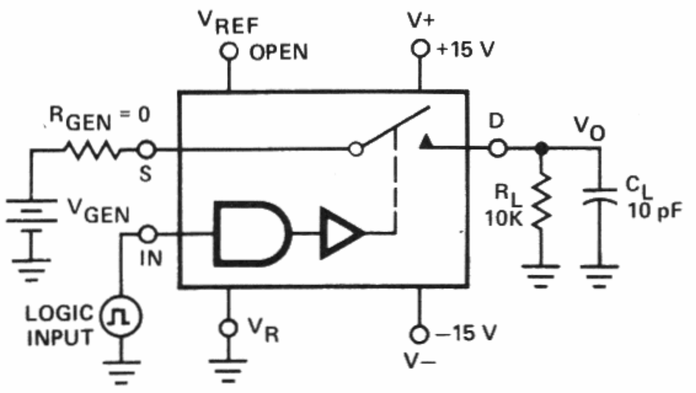


Supply Current vs Temperature

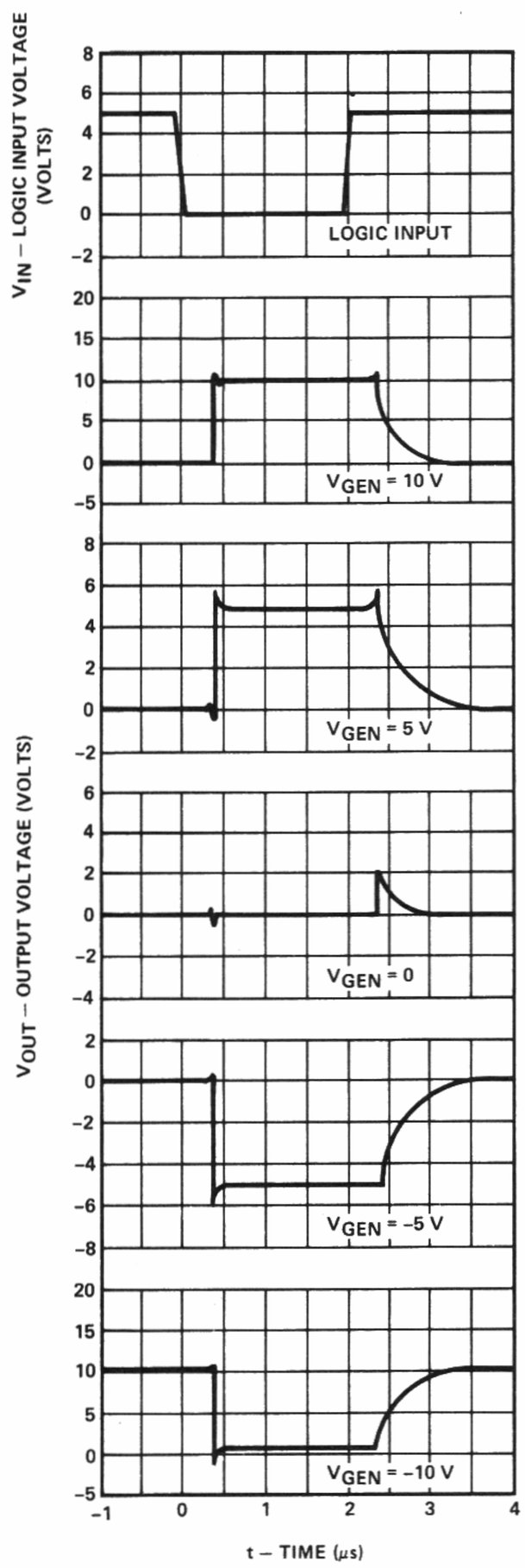


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuit.

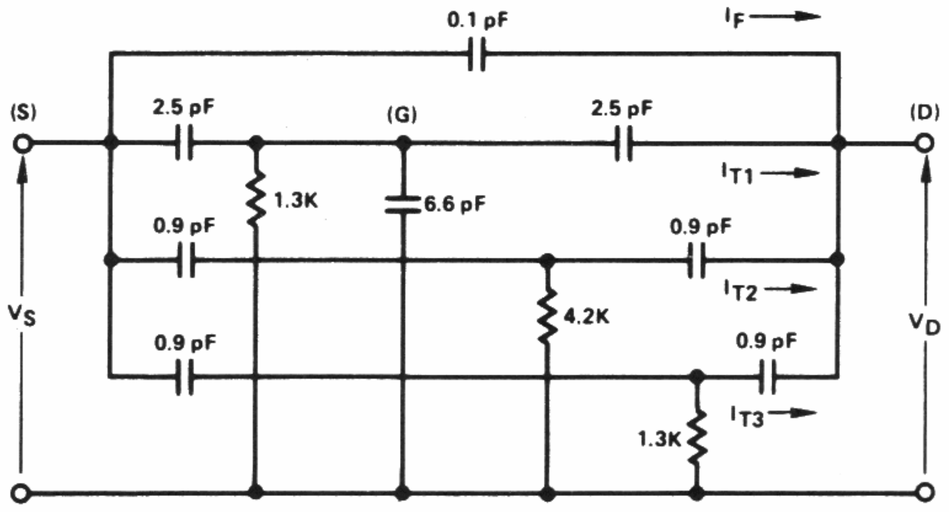


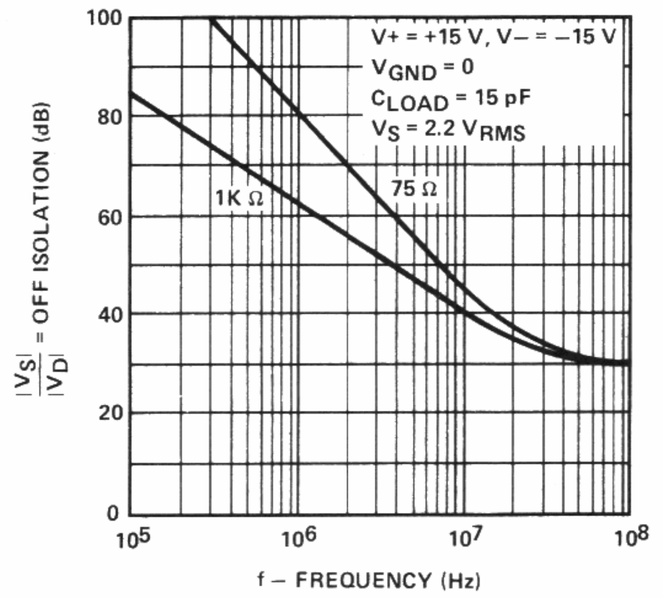
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.



TYPICAL CHARACTERISTICS (Cont'd)

"OFF" Isolation Equivalent Circuit and Data

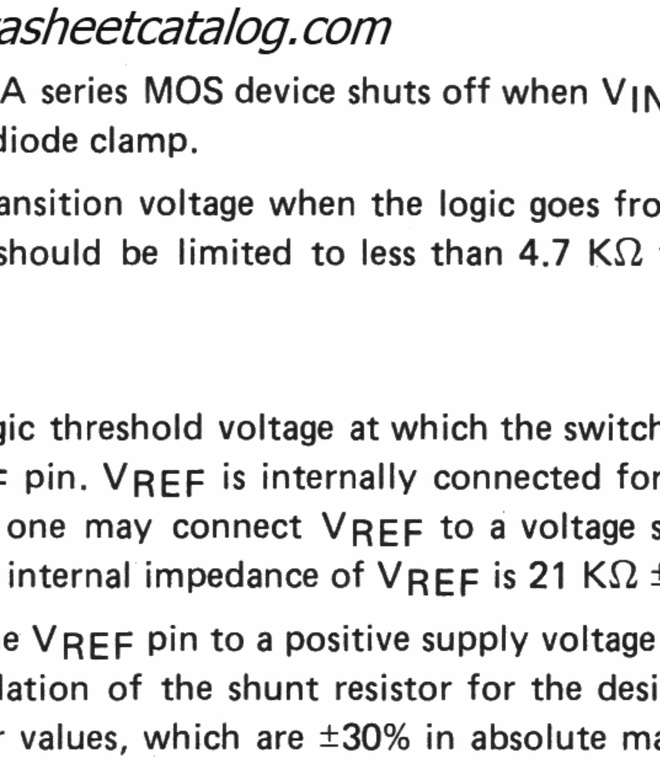




APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	–15	Open	2.4/0.8	–15 to +15
+12	–12	Open or 1.4 V	2.4/0.8	–12 to +12
+10	–10	1.4 V	2.4/0.8	–10 to +10
+8***	–8	1.4 V	2.4/0.8	–8 to +8



*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V– = –15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 4.7 KΩ to insure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin. V_{REF} is internally connected for a 1.4 V threshold at V+ = +15 V. For other thresholds and/or supply voltages, one may connect V_{REF} to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21 KΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5 V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{\left[R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)\right]}$$

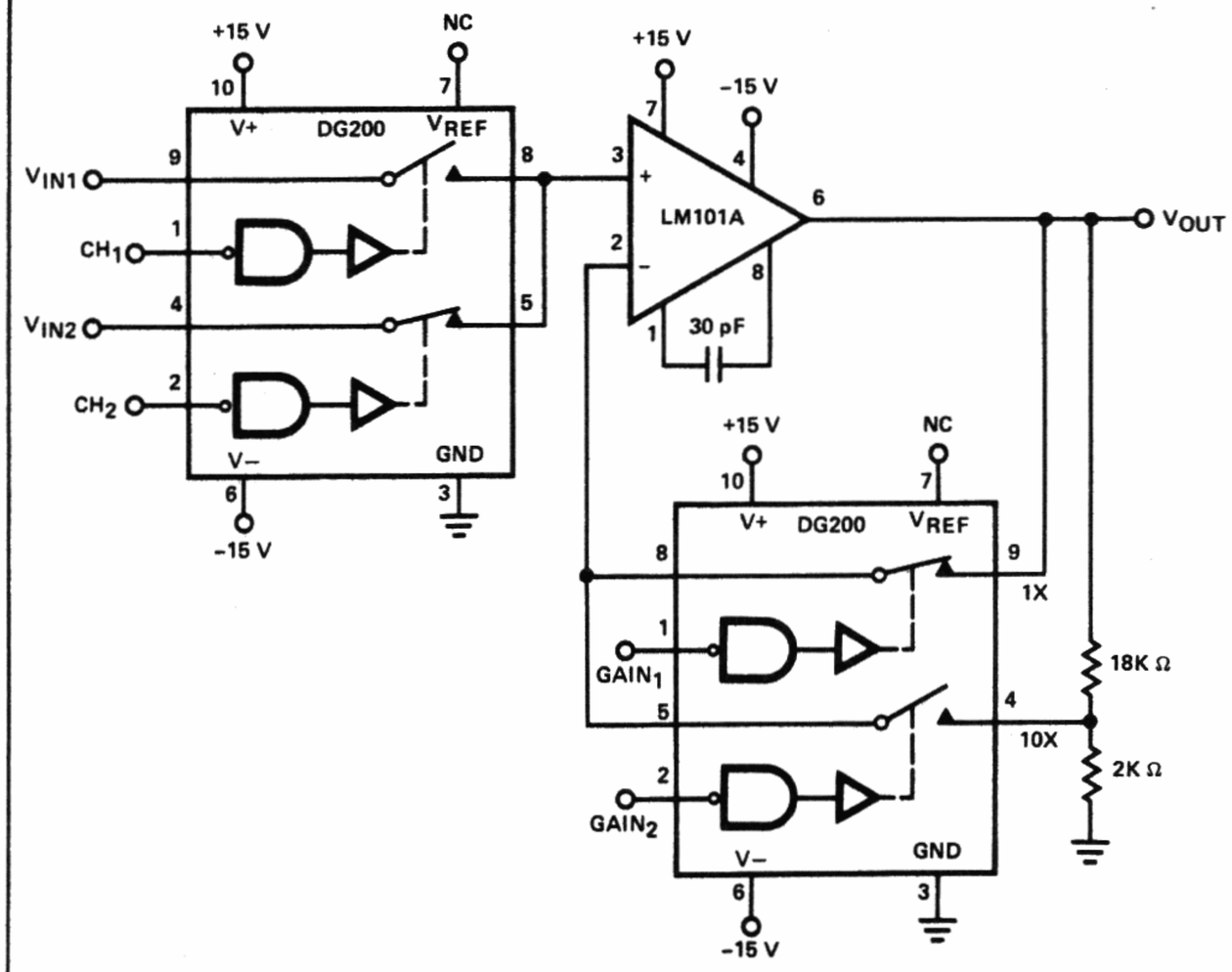
Calculation of R_{SHUNT}

Where $R1 \simeq 220$ KΩ: nominal values,
$R2 \simeq 23$ KΩ ±30% run to run

Example: for V+ = 15 V, V_{TRIP} = 5 V, using nominal R1, R2 calc R_{SHUNT} = 58 KΩ.

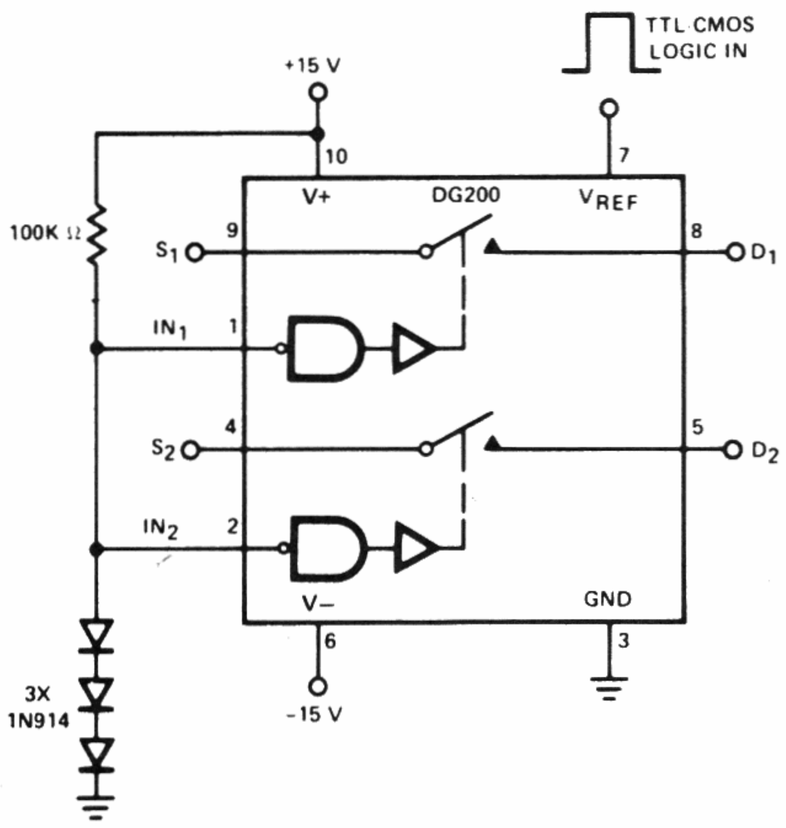
APPLICATIONS (Cont'd)

Programmable Gain Non-Inverting Amplifier with Selectable Inputs



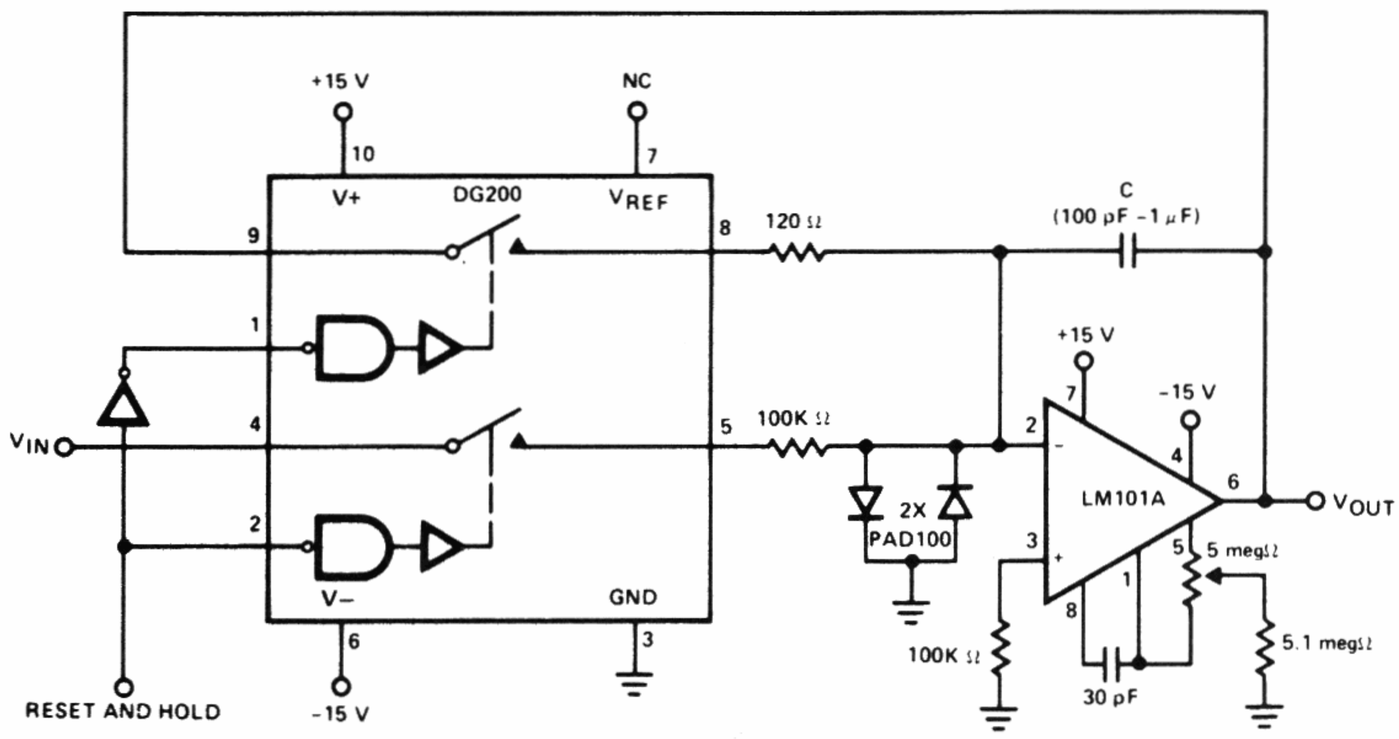
Non-Inverted Operation (Logic 1 = ON)

Can be used with a second DG200 connected in the standard way to make a DPDT without the need for an additional inverter.



NOTE: Both channels switch simultaneously

Integrator Reset

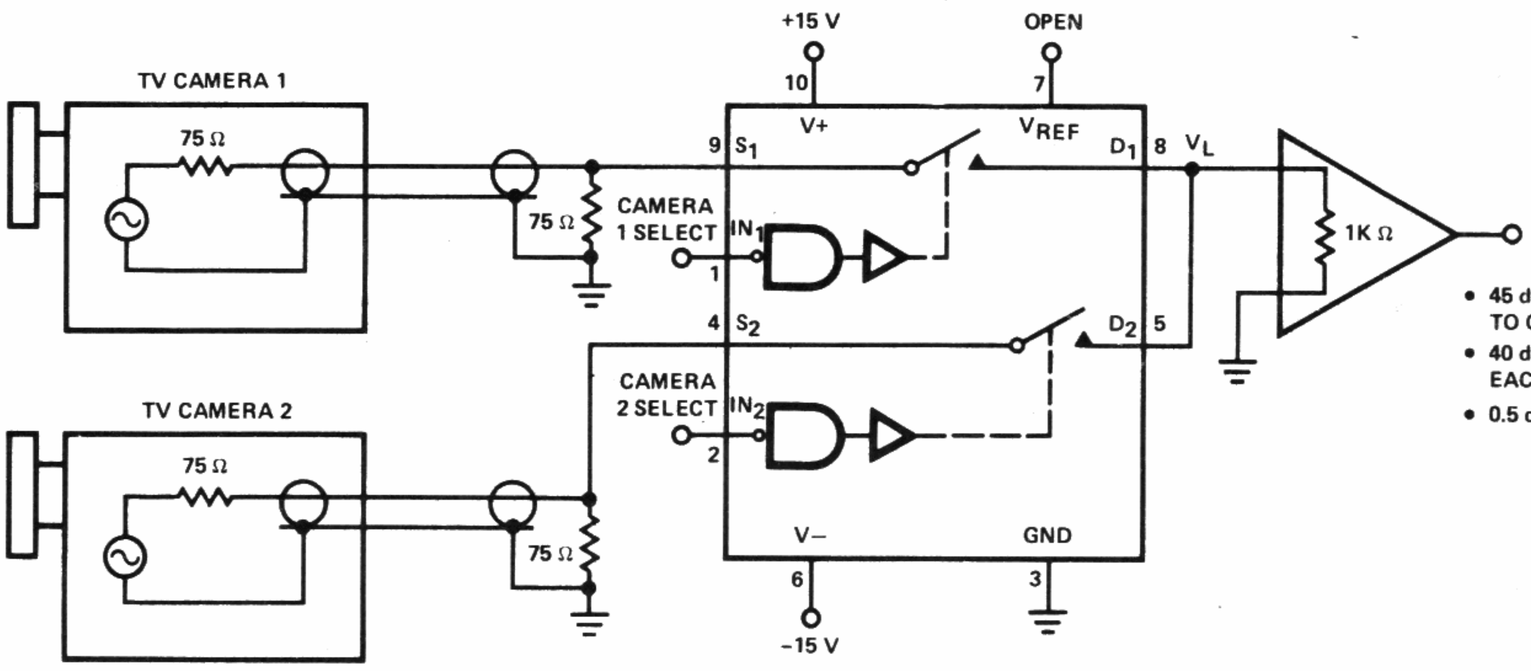


$$V_O = \frac{10}{C}\int_{t_1}^{t_2} V_{IN}\,dt \qquad (C \text{ in } \mu F)$$

NOTE: Pin connections shown for metal can package

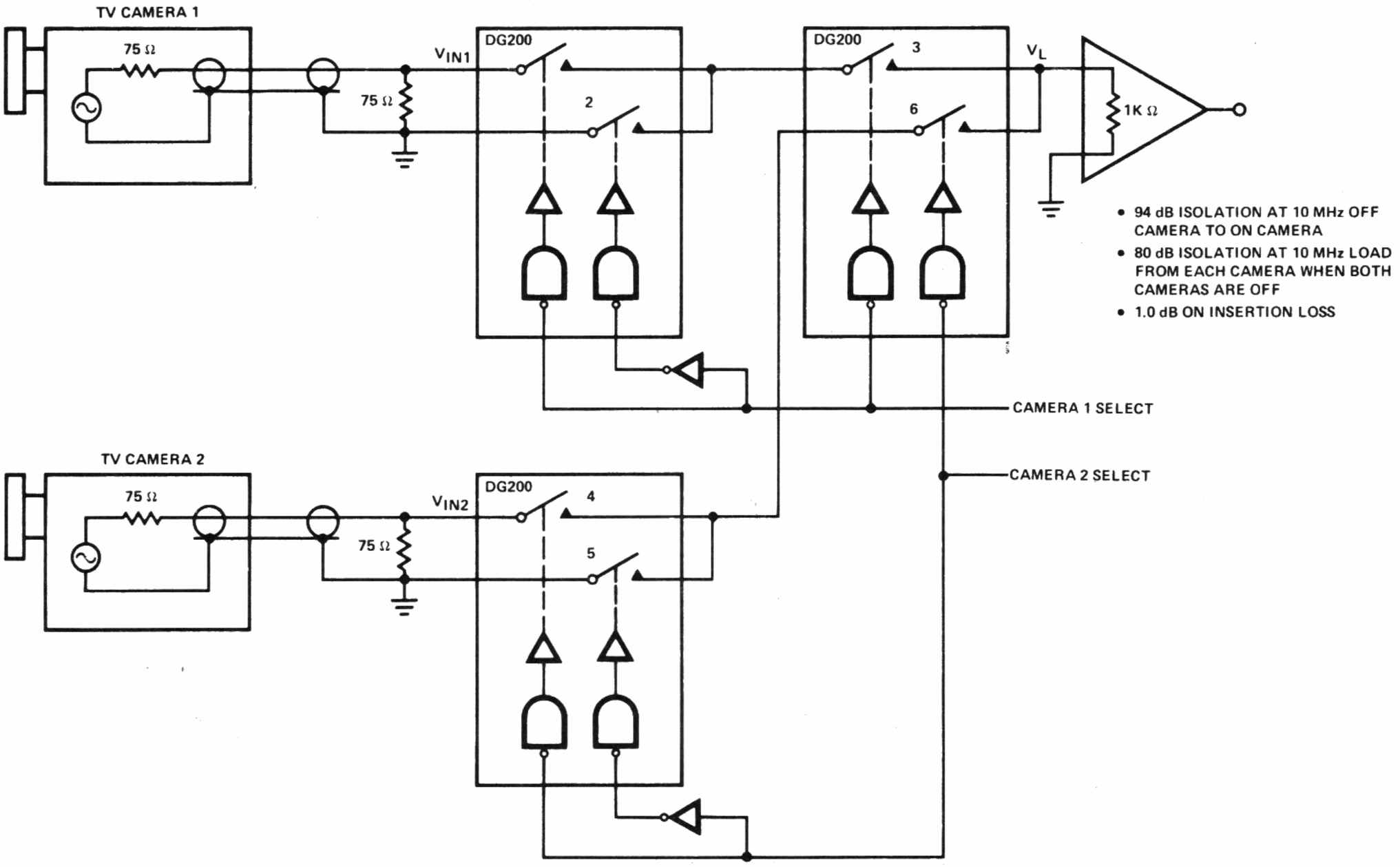
APPLICATIONS (Cont'd)

VIDEO SWITCH
(f = DC to 10 MHz)



- 45 dB ISOLATION Δ T 10 MHz OFF CAMERA TO ON CAMERA
- 40 dB ISOLATION AT 10 MHz, LOAD FROM EACH CAMERA WHEN BOTH ARE OFF
- 0.5 dB ON INSERTION LOSS

VIDEO SWITCH WITH VERY HIGH OFF ISOLATION
(f = DC to 10 MHz)



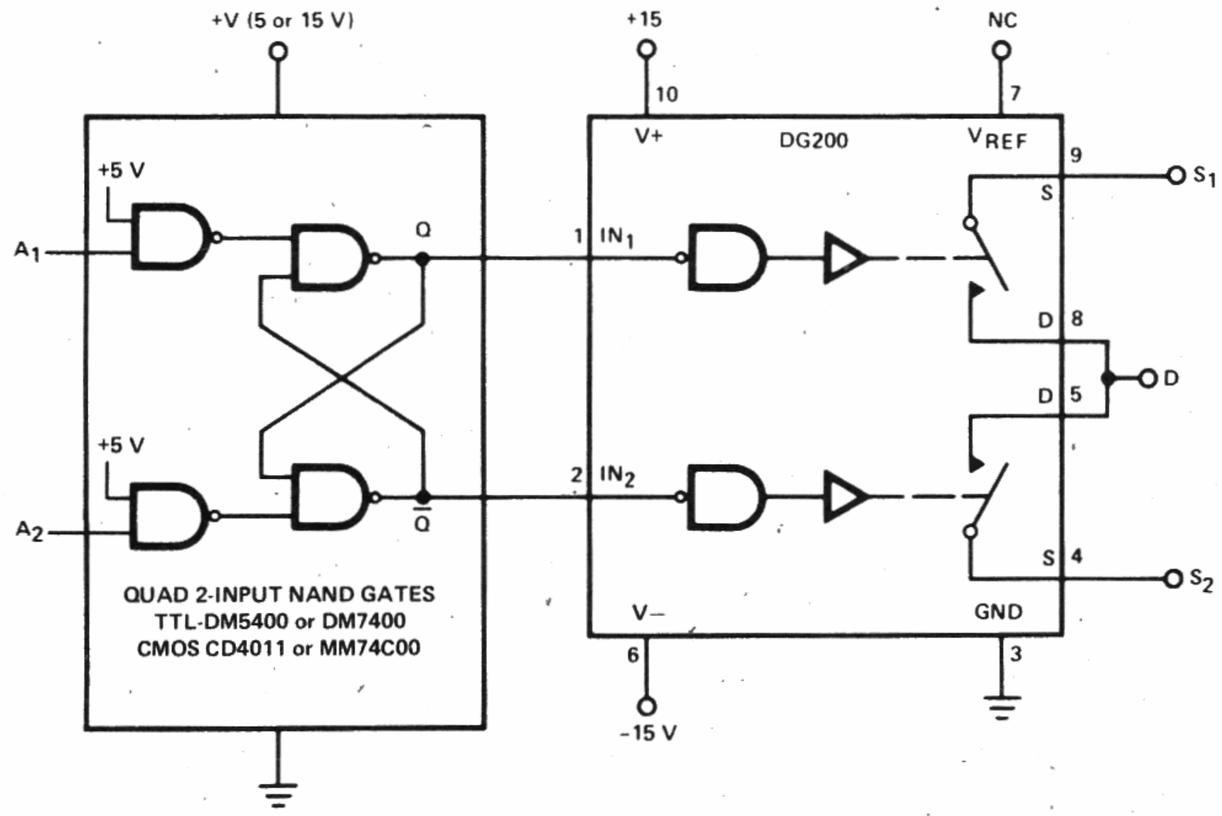
- 94 dB ISOLATION AT 10 MHz OFF CAMERA TO ON CAMERA
- 80 dB ISOLATION AT 10 MHz LOAD FROM EACH CAMERA WHEN BOTH CAMERAS ARE OFF
- 1.0 dB ON INSERTION LOSS

NOTE: Pin connections shown are for metal can package

APPLICATIONS (Cont'd)

A Latching SPDT

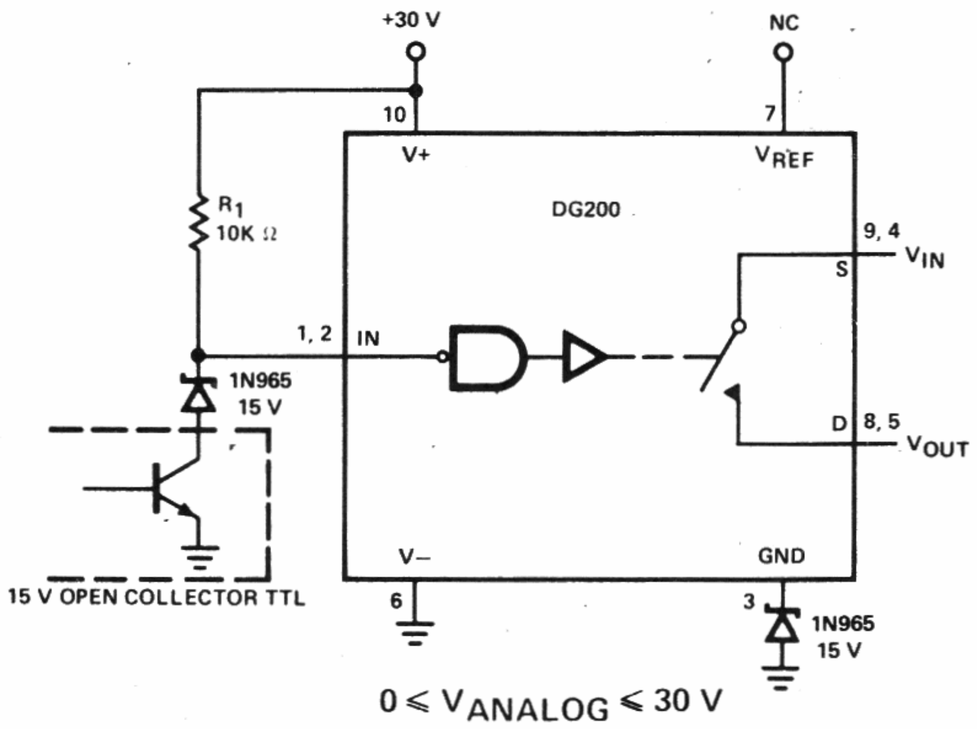
The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_1 turns S_2 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



TRUTH TABLE

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_2	S_1
0	0 (normal)	same	same
0	1	ON	OFF
1	0	OFF	ON
1	1	INDETERMINATE	

Operation From a Unipolar Supply



$0 \leqslant V_{ANALOG} \leqslant 30\ V$

NOTE: Pin connections shown for metal can package

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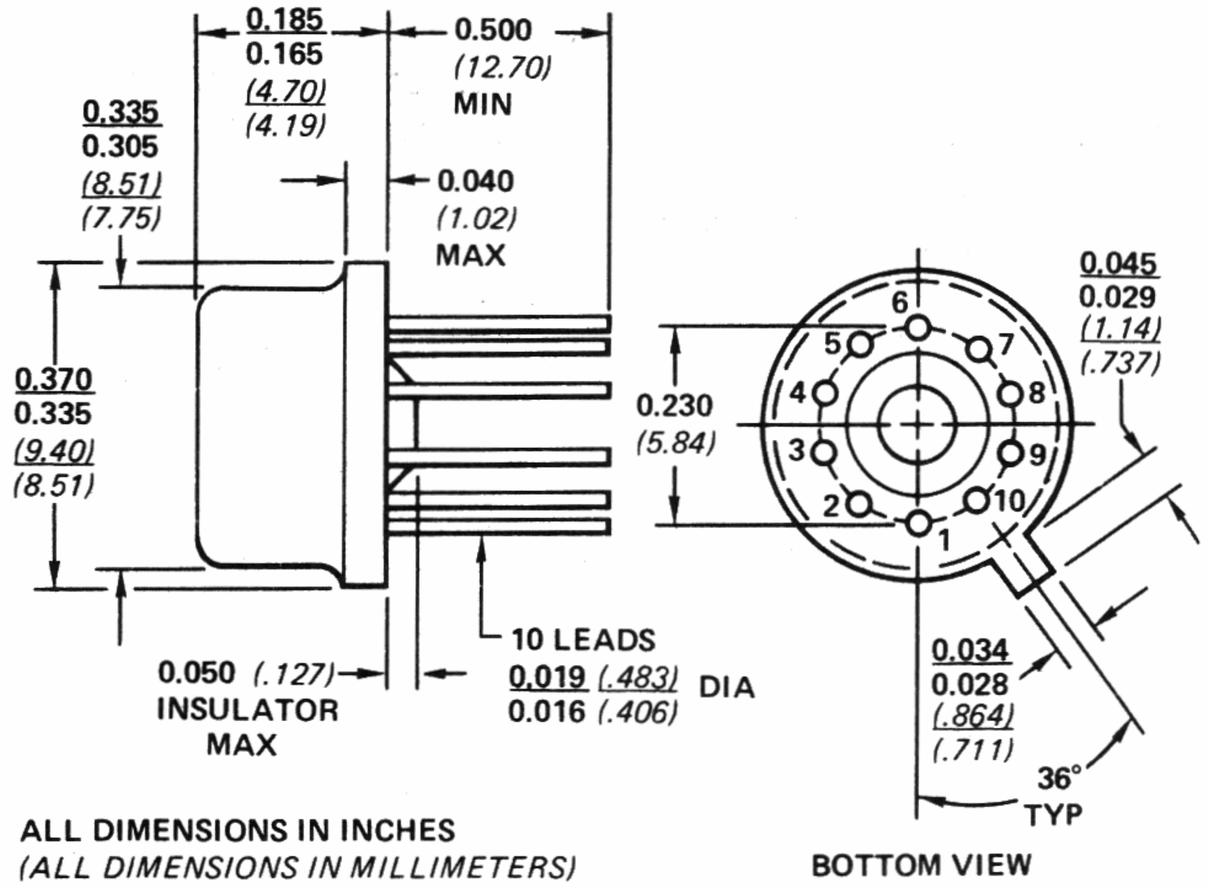

PACKAGE 2
10 LEAD TO-100 TYPE METAL CAN **(A)**