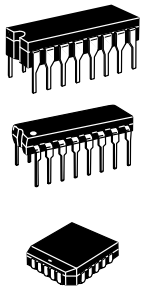
Quad MECL to TTL Translator

MC10125

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ non–inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single–ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and –5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.



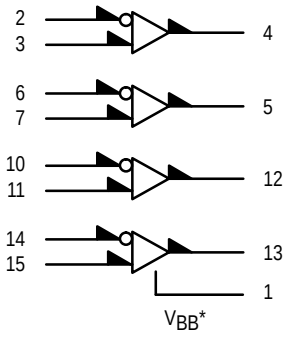
L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

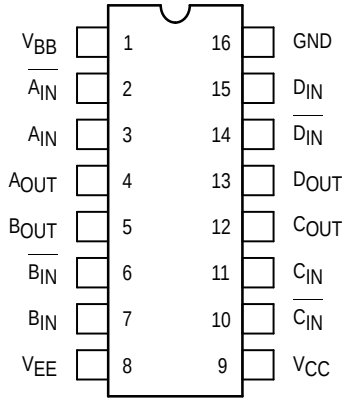
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to + 1.5 Vdc out)
t_r, t_f = 2.5 ns typ (1.0 V to 2.0 V)

LOGIC DIAGRAM



Gnd = PIN 16
V_{CC} (+5.0Vdc) = PIN 9
V_{EE} (–5.2Vdc) = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

*V_{BB} to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8		–44			–40		–44	mAdc
Positive Power Supply Drain Current	I_{CCH}	9		52			52		52	mAdc
	I_{CCL}	9		39			39		39	mAdc
Input Current	I_{inH}[1]	2		180			115		115	μAdc
Input Leakage Current	I_{CBO}	2		1.5			1.0		1.0	μAdc
High Output Voltage	V_{OH}	4	2.5		2.5			2.5		Vdc
Low Output Voltage	V_{OL}	4		0.5			0.5		0.5	Vdc
High Threshold Voltage	V_{OHA}	4	2.5		2.5			2.5		Vdc
Low Threshold Voltage	V_{OLA}	4		0.5			0.5		0.5	Vdc
Indeterminate Input Protection Tests	V_{OLS1}	4		0.5			0.5		0.5	Vdc
	V_{OLS2}	4		0.5			0.5		0.5	Vdc
Short Circuit Current	I_{OS}	4	40	100	40		100	40	100	mAdc
Reference Voltage	V_{BB}	1	–1.420	–1.280	–1.350		–1.230	–1.295	–1.150	Vdc
Common Mode Rejection Tests	V_{OH}	4 4	2.5 2.5		2.5 2.5			2.5 2.5		Vdc
	V_{OL}	4 4		0.5 0.5			0.5 0.5		0.5 0.5	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay (50% to +1.5Vdc)	t_{6+5-} t_{6-5+} t_{2+4-} t_{2-4+}	5 5 4 4	1.0 1.0 1.0 1.0	6.0 6.0 6.0 6.0	1.0 1.0 1.0 1.0	4.5 4.5 4.5 4.5	6.0 6.0 6.0 6.0	1.0 1.0 1.0 1.0	6.0 6.0 6.0 6.0	
Rise Time (+1.0V to 2.0V)	t_{4+}	4		3.3			3.3		3.3	
Fall Time (+1.0V to 2.0V)	t_{4-}	4		3.3			3.3		3.3	

1. Individually test each output, apply V_{IHmax} to pin under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)							
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}		
–30°C	–0.890	–1.890	–1.205	–1.500	+0.110	–0.890		
+25°C	–0.810	–1.850	–1.105	–1.475	+0.190	–0.850		
+85°C	–0.700	–1.825	–1.035	–1.440	+0.300	–0.825		

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd	Output Condition
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}		
Negative Power Supply Drain Current	I_E	8							16	
Positive Power Supply Drain Current	I_{CCH}	9	2,6,10,14						16	
	I_{CCL}	9		2,6,10,14					16	
Input Current	I_{inH}[1]	2	2,6,10,14						16	
Input Leakage Current	I_{CBO}	2							16	
High Output Voltage	V_{OH}	4		2,6,10,14					16	–2.0mA
Low Output Voltage	V_{OL}	4	2,6,10,14						16	20mA
High Threshold Voltage	V_{OHA}	4		6,10,14		2			16	–2.0mA
Low Threshold Voltage	V_{OLA}	4	6,10,14		2				16	20mA
Indeterminate Input Protection Tests	V_{OLS1}	4							16	20mA
	V_{OLS2}	4							16	20mA
Short Circuit Current	I_{OS}	4		2,6,10,14					4, 16	
Reference Voltage	V_{BB}	1		2,6,10,14						
Common Mode Rejection Tests	V_{OH}	4 4					3	2	16 16	–2.0mA –2.0mA
	V_{OL}	4 4					2	3	16 16	20mA 20mA
Switching Times (50Ω Load)			**Pulse In**	**Pulse Out**	**C_L** (pF)					
Propagation Delay (50% to +1.5Vdc)	t_{6+5-}	5	6	5	25				16	
	t_{6-5+}	5	6	5	25				16	
	t_{2+4-}	4	2	4	25				16	
	t_{2-4+}	4	2	4	25				16	
Rise Time (+1.0V to 2.0V)	t_{4+}	4	2	4	25				16	
Fall Time (+1.0V to 2.0V)	t_{4-}	4	2	4	25				16	

1. Individually test each output, apply V_{IHmax} to pin under test.

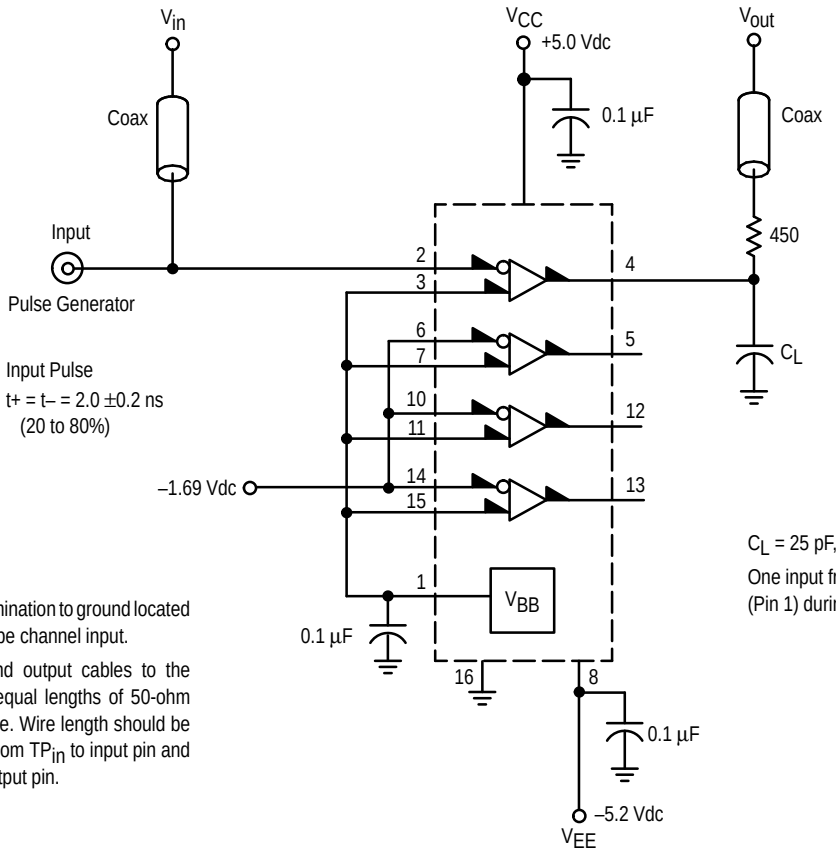
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts) V_{IHH}	V_{ILH}	V_{BB}	V_{CC}	V_{EE}		
–30°C			–1.890	–2.890	From Pin 1	+5.0	–5.2		
+25°C			–1.810	–2.850		+5.0	–5.2		
+85°C			–1.700	–2.825		+5.0	–5.2		
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW** V_{IHH}	V_{ILH}	V_{BB}	V_{CC}	V_{EE}	**Gnd**	**Output Condition**
Negative Power Supply Drain Current	I_E	8			3,7,11,15	9	8	16	
Positive Power Supply Drain Current	I_{CCH}	9			3,7,11,15	9	8	16	
	I_{CCL}	9			3,7,11,15	9	8	16	
Input Current	I_{inH}[1]	2			3,7,11,15	9	8	16	
Input Leakage Current	I_{CBO}	2			3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V_{OH}	4			3,7,11,15	9	8	16	–2.0mA
Low Output Voltage	V_{OL}	4			3,7,11,15	9	8	16	20mA
High Threshold Voltage	V_{OHA}	4			3,7,11,15	9	8	16	–2.0mA
Low Threshold Voltage	V_{OLA}	4			3,7,11,15	9	8	16	20mA
Indeterminate Input Protection Tests	V_{OLS1}	4				9	2,3,6,7,8, 10,11,14,15	16	20mA
	V_{OLS2}	4				9	8	16	20mA
Short Circuit Current	I_{OS}	4			3,7,11,15	9	8	4, 16	
Reference Voltage	V_{BB}	1			3,7,11,15				
Common Mode Rejection Tests	V_{OH}	4				9	8	16	–2.0mA
		4	3	2		9	8	16	–2.0mA
	V_{OL}	4				9	8	16	20mA
		4	2	3		9	8	16	20mA
Switching Times (50Ω Load)									
Propagation Delay (50% to +1.5Vdc)	t_{6+5-}	5			3,7,11,15	9	8	16	
	t_{6-5+}	5			3,7,11,15	9	8	16	
	t_{2+4-}	4			3,7,11,15	9	8	16	
	t_{2-4+}	4			3,7,11,15	9	8	16	
Rise Time (+1.0V to 2.0V)	t_{4+}	4			3,7,11,15	9	8	16	
Fall Time (+1.0V to 2.0V)	t_{4-}	4			3,7,11,15	9	8	16	

1. Individually test each output, apply V_{IHmax} to pin under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

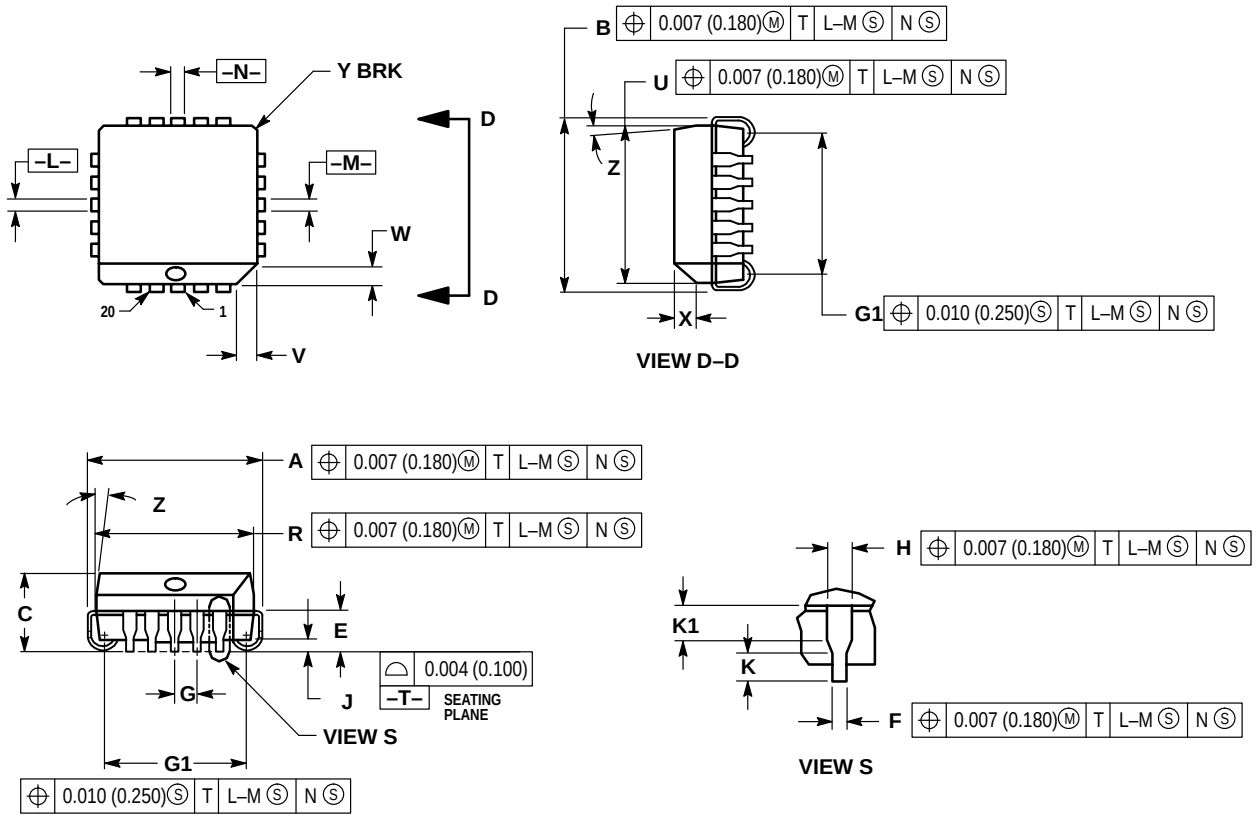
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Pin 1) during testing.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

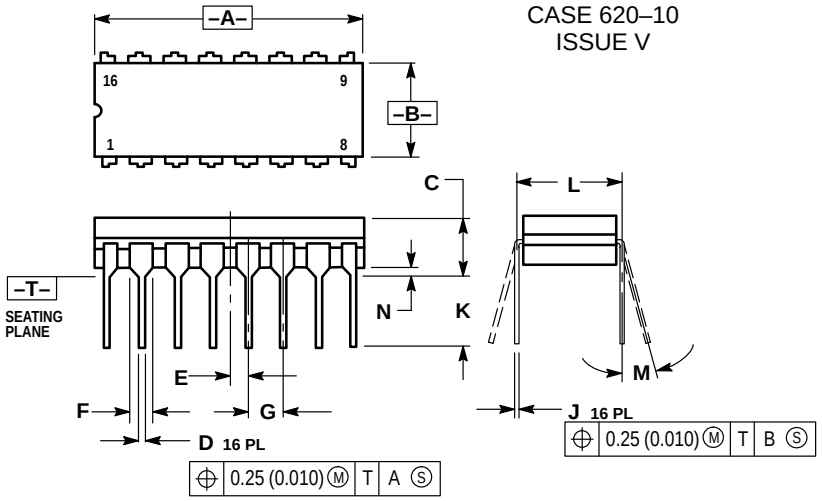


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

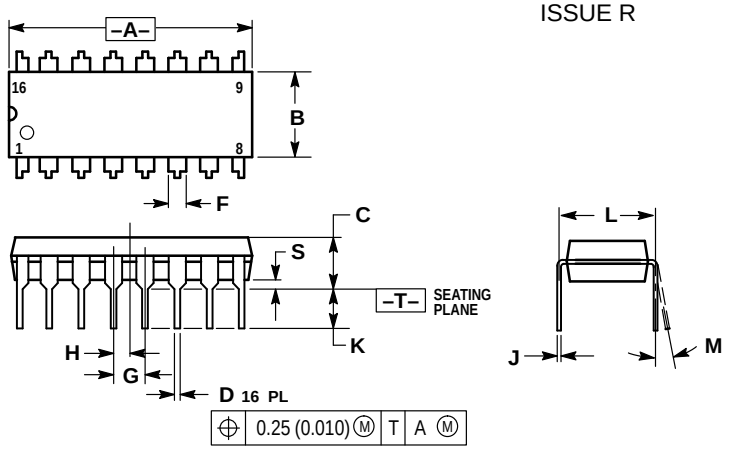
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

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