



MUX-08/MUX-24

8-CHANNEL/DUAL 4-CHANNEL JFET ANALOG MULTIPLEXERS (OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED)

Precision Monolithics Inc.

FEATURES

- JFET Switches Rather Than CMOS
- Low "ON" Resistance 220Ω Typ
- Highly Resistant to Static Discharge Damage
- No SCR Latch-Up Problems
- Digital Inputs Compatible With TTL and CMOS
- 125°C Temperature Tested Dice Available
- MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506
- MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507
- Available in Surface Mount Packages
- Available in Die Form

ORDERING INFORMATION †

25°C ON RESISTANCE	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 16-PIN	PLASTIC 16-PIN	LCC 20-CONTACT	
220Ω	MUX08AQ*	-	-	MIL
	MUX08EQ	-	-	IND
	-	MUX08EP	-	COM
300Ω	MUX08BQ*	-	MUX08BRC/883	MIL
	MUX08FQ	-	-	IND
	-	MUX08FP	-	XIND
		MUX08FS††	-	XIND
220Ω	MUX24AQ*	-	-	MIL
	MUX24EQ	-	-	IND
	-	MUX24EP	-	COM
300Ω	MUX24BQ*	-	-	MIL
	MUX24FQ	-	-	IND
	-	MUX24FP	-	XIND
		MUX24FS††	-	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

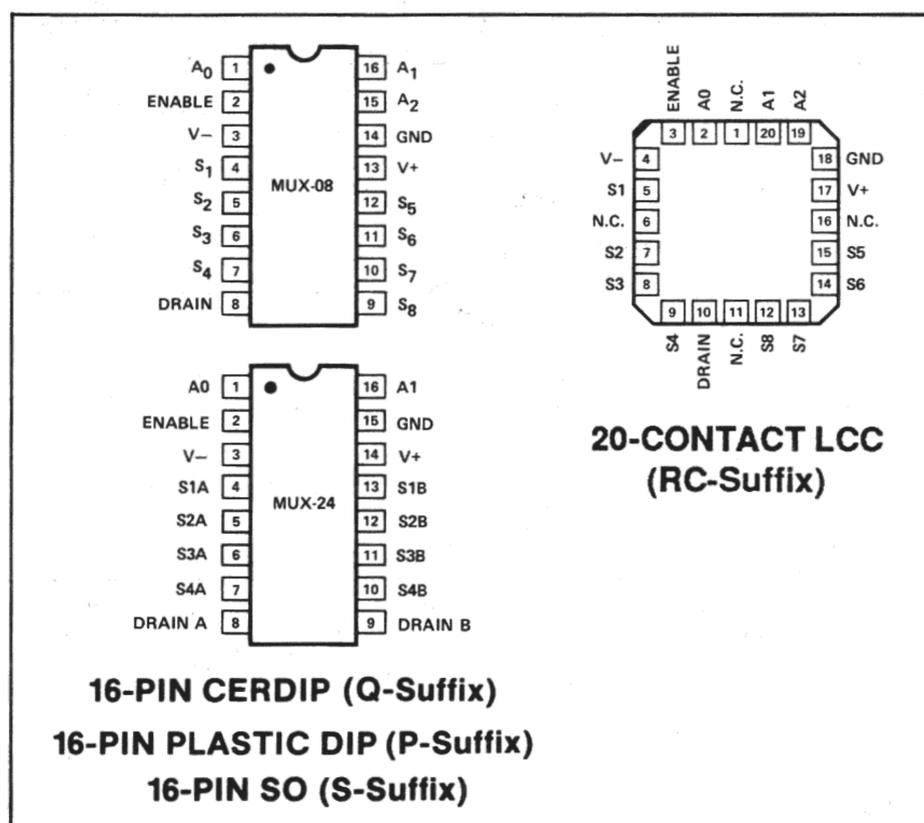
All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time

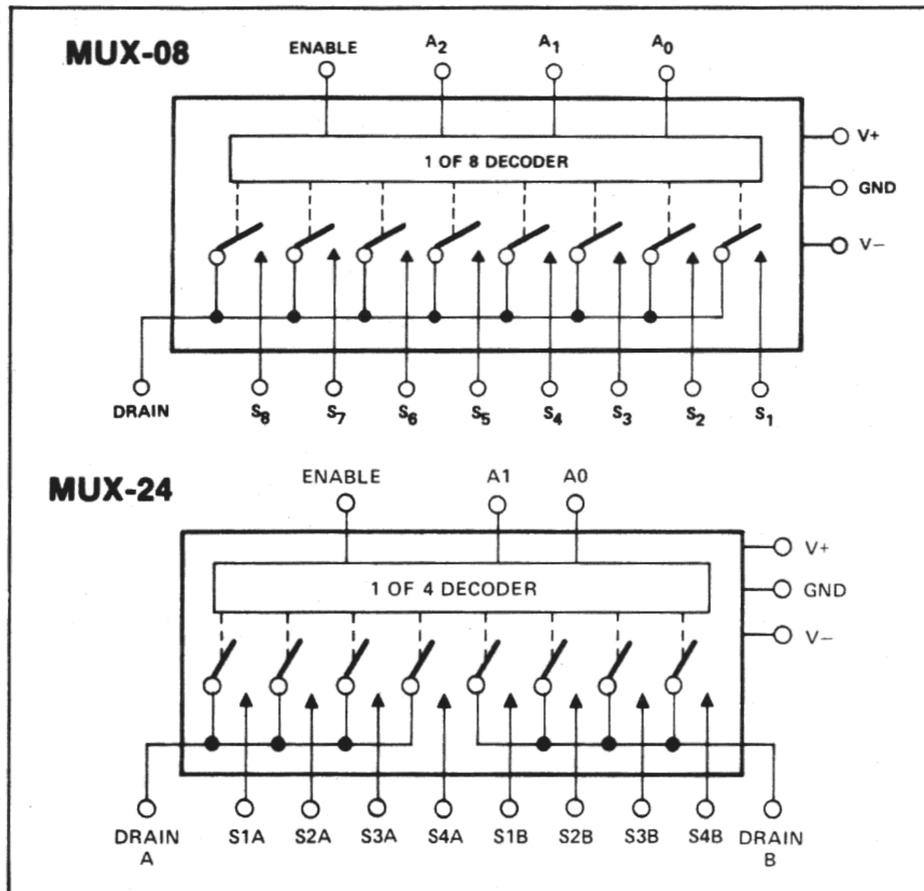
with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

PIN CONNECTIONS



FUNCTIONAL DIAGRAMS





ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
 MUX-08/24-AQ, BQ, BRC -55°C to +125°C
 MUX-02/24-EQ, FQ -25°C to +85°C
 MUX-08/24-EP 0°C to +70°C
 MUX-08/24-FP, FS -40°C to +85°C
 Junction Temperature (T_j) -65°C to +150°C
 Storage Temperature Range -65°C to +150°C
 P-Suffix -65°C to +125°C
 Lead Temperature (Soldering, 60 sec) 300°C
 Maximum Junction Temperature 150°C
 V+ Supply to V- Supply 36V
 Logic Input Voltage (-4V or V-) to V+ Supply

Analog Input Voltage V- Supply -20V to V+ Supply +20V
 Maximum Current Through Any Pin 25mA

PACKAGE TYPE	θ _{JA} (Note 2)	θ _{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/E MUX-24A/E			MUX-08B/F MUX-24B/F			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R _{ON}	V _S ≤ 10V, I _S ≤ 200μA	—	220	300	—	300	400	Ω	
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200μA	—	1	5	—	3	7	%	
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 200μA	—	7	15	—	9	20	%	
Analog Voltage Range	V _A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V	
Source Current (Switch "OFF")	I _{S(OFF)}	V _S = 10V, V _D = -10V (Note 1)	—	0.01	1.0	—	0.01	2.0	nA	
Drain Current (Switch "OFF")	I _{D(OFF)}	V _S = 10V, V _D = -10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	I _{D(ON)} + I _{S(ON)}	V _D = 10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Digital Input Current	I _{IN}	V _{IN} = 0.4V to 15V	—	1	10	—	1	10	μA	
Digital "0" Enable Current	I _{INL(EN)}	V _{EN} = 0.4V	—	4	10	—	4	10	μA	
Digital Input Capacitance	C _{DIG}		—	3	—	—	3	—	pF	
Switching Time (t _{TRAN})	t _{PHL}	(Notes 2, 5) Figure 1	—	1.5	2.1	—	1.5	2.1	μs	
	t _{PLH}	(Test Circuit)	—	1.0	1.3	—	1.0	1.3		
Output Settling Time	t _S	10V Step to 0.10%	—	2.2	—	—	2.2	—	μs	
		10V Step to 0.05%	—	2.7	—	—	2.7	—		
		10V Step to 0.02%	—	3.4	—	—	3.4	—		
Break-Before-Make Delay	t _{OPEN}	Figure 3 (Test Circuit)	—	0.8	—	—	1.0	—	μs	
Enable Delay "ON"	t _{ON(EN)}	(Note 5) Figure 2 (Test Circuit)	—	1	2	—	1	2	μs	
Enable Delay "OFF"	t _{OFF(EN)}	(Note 5) Figure 2 (Test Circuit)	MUX-08	—	0.1	0.4	—	0.2	0.4	μs
			MUX-24	—	0.2	0.5	—	0.3	0.6	
"OFF" Isolation	ISO _{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— —	60 66	— —	60 66	— —	dB	
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08	—	70	—	—	70	—	dB
			MUX-24	—	76	—	—	76	—	
Source Capacitance	C _{S(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08	—	2.5	—	—	2.5	—	pF
			MUX-24	—	2	—	—	2	—	
Drain Capacitance	C _{D(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08	—	7	—	—	7	—	pF
			MUX-24	—	4	—	—	4	—	
Input to Output Capacitance	C _{DS(OFF)}	(Note 4)	MUX-08	—	0.3	—	—	0.3	—	pF
			MUX-24	—	0.15	—	—	0.15	—	
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I ₊	V ₊ = 15V	—	10	12	—	6	12	mA	
		V ₊ = 5V	—	8	—	—	5	—		
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I ₋	V ₊ = -15V	—	3.0	3.8	—	2.0	3.8	mA	
		V ₊ = -5V	—	2.5	—	—	1.8	—		

ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/ MUX-24A			MUX-08B/ MUX-24B			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	400	—	—	500	Ω	
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%	
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	25	—	—	50	nA	
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —		500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+ I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —		500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V	
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA	
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA	
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA	
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA	

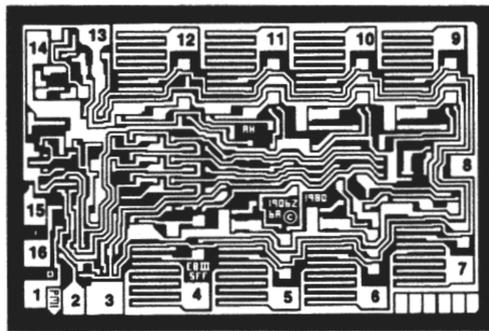
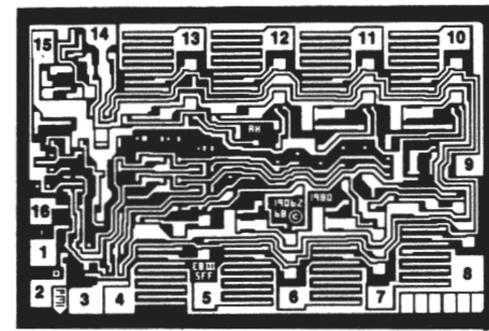
ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $-25^\circ C \leq T_A \leq +85^\circ C$ for MUX-08EQ/FQ and MUX-24EQ/FQ; $0^\circ C \leq T_A \leq +70^\circ C$ for MUX-08EP and MUX-24EP; $-40^\circ C \leq T_A \leq +85^\circ C$ for MUX-08FP/FS and MUX-24FP/FS, unless otherwise noted.

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PARAMETER	SYMBOL	CONDITIONS	MUX-08E/ MUX-24E			MUX-08F/ MUX-24F			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	400	—	—	500	Ω	
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%	
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	10	—	—	10	nA	
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —		100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+ I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —		100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V	
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	—	—	0.8	V	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA	
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA	
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA	
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA	

NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- $R_L = 10M\Omega$, $C_L = 10pF$.
- Crosstalk is measured by driving channel 8 with channel 4 "ON".
 $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$.
- "OFF" isolation is measured by driving channel 8 with ALL channels "OFF".
 $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$. C_{DS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.
- Leakage tests are performed only on military temperature grades at 125°C.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

MUX-08
MUX-24

**DIE SIZE 0.093 × 0.059 inch, 5487 sq. mils
(2.362 × 1.500 mm, 3543 sq. mm)**

- | | |
|-------------------|---------|
| 1. A0 | 9. S8 |
| 2. ENABLE | 10. S7 |
| 3. V- (SUBSTRATE) | 11. S6 |
| 4. S1 | 12. S5 |
| 5. S2 | 13. V+ |
| 6. S3 | 14. GND |
| 7. S4 | 15. A2 |
| 8. DRAIN | 16. A1 |

- | | |
|-------------------|------------|
| 1. A0 | 9. DRAIN B |
| 2. ENABLE | 10. S4 B |
| 3. V- (SUBSTRATE) | 11. S3 B |
| 4. S1 A | 12. S2 B |
| 5. S2 A | 13. S1 B |
| 6. S3 A | 14. V+ |
| 7. S4 A | 15. GND |
| 8. DRAIN A | 16. A1 |

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 200\mu A$ $T_A = 125^\circ C$	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V_{INH}	(Note 2)	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}	(Note 2)	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$ $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{IN} = 0.4V$ $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I_+	$T_A = 125^\circ C$	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I_-	$T_A = 125^\circ C$	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V_A	(Note 2)	± 10	± 10	± 10	V MIN

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$ for MUX-08/24N & G, $T_A = 125^\circ C$ for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL}	(Note 1)	1.7	1.3	2.1	μS
	t_{PLH}	(Note 1)	1.1	0.9	1.3	μS
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	μS
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	μS
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	2	2	6	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+10.4/-15	+10.4/-15	+10.4/-15	V

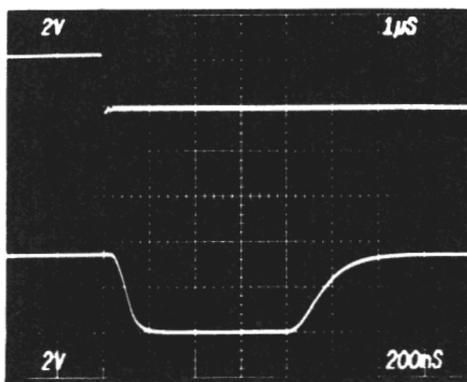
NOTES:
 1. The data shown is extrapolated from measurements made on the packaged devices.
 2. Guaranteed by leakage current and R_{ON} tests.

**MUX-08
LOGIC STATE**

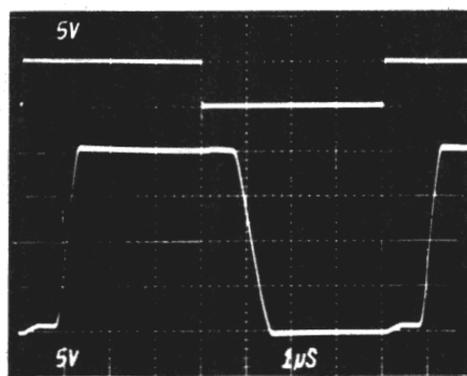
A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

**MUX-24
LOGIC STATE**

A ₁	A ₀	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)
**MUX-08
BREAK-BEFORE-MAKE
SWITCHING**


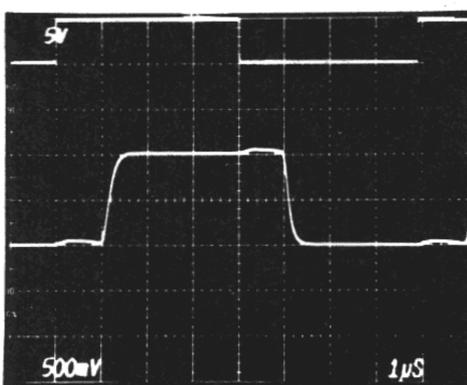
$R_L = 1k\Omega$, $C_L = 10pF$, $V_1, 8 = 10V$
 VOLTAGE = 2V/DIV
 TIME = 200ns/DIV

**MUX-08
LARGE-SIGNAL SWITCHING**


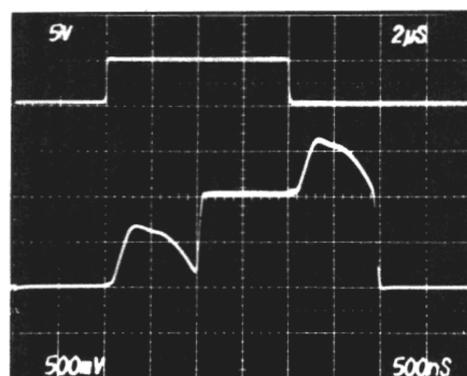
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_8 = +10V$
 VOLTAGE = 5V/DIV
 TIME = 1μs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING**

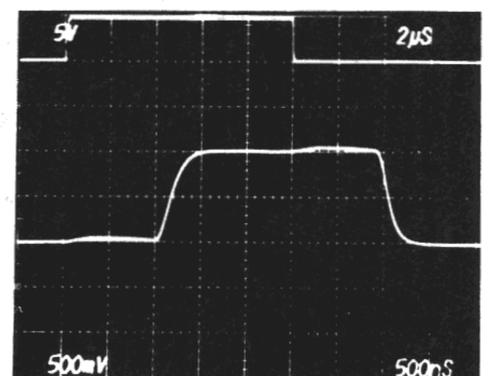

$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$, $V_8 = +500mV$
 VOLTAGE = 500mV/DIV
 TIME = 1μs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING**


$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = 500mV$, $V_8 = +500mV$
 VOLTAGE = 500mV/DIV
 TIME = 1μs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH 2μs SAMPLE TIME**


$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$, $V_8 = +500mV$
 VOLTAGE = 500mV/DIV
 TIME = 500ns/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING AND
2.5μs SAMPLE TIME**


$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$, $V_8 = +500mV$
 VOLTAGE = 500mV/DIV
 TIME = 500ns/DIV

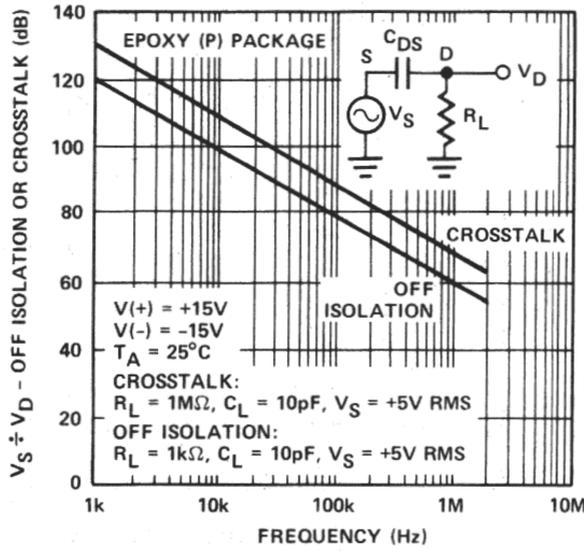
NOTE:

Top waveforms: Digital Input 5V/DIV
 Bottom waveforms: Multiplexer Output

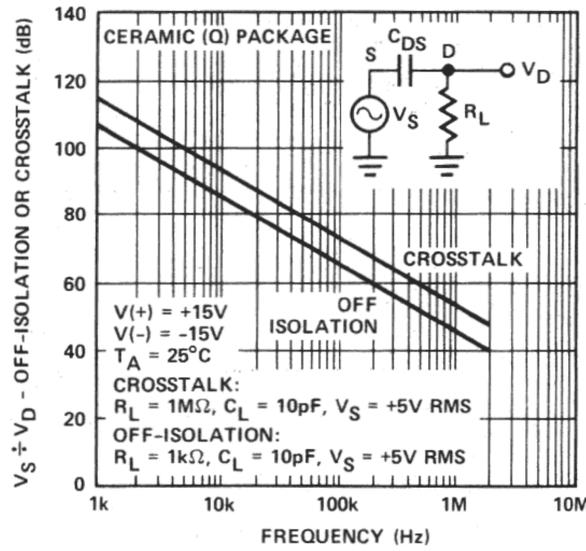
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TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

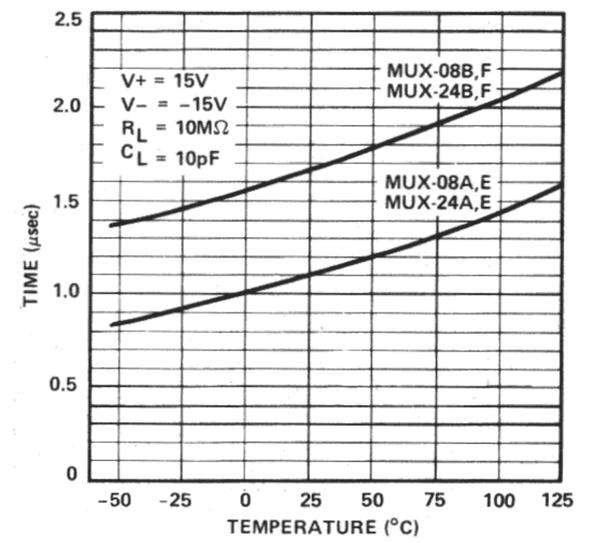
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8

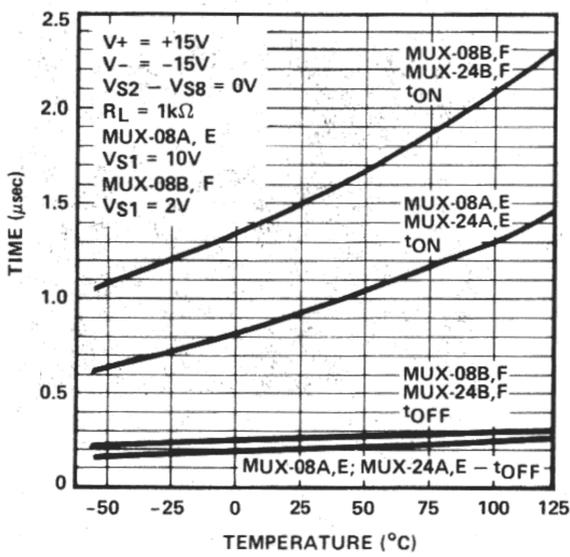


TRANSITION TIMES vs TEMPERATURE

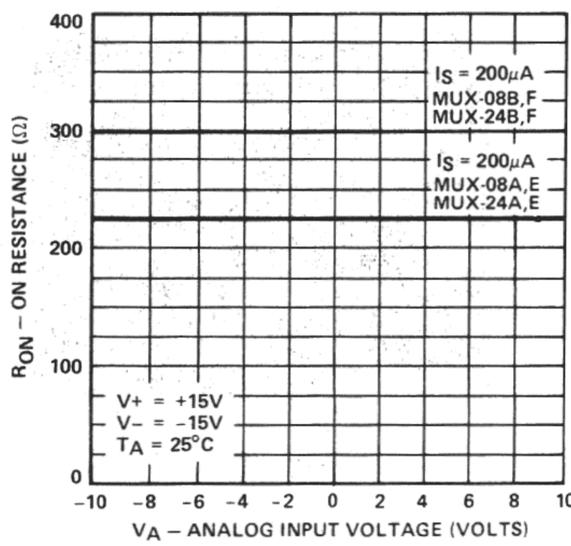


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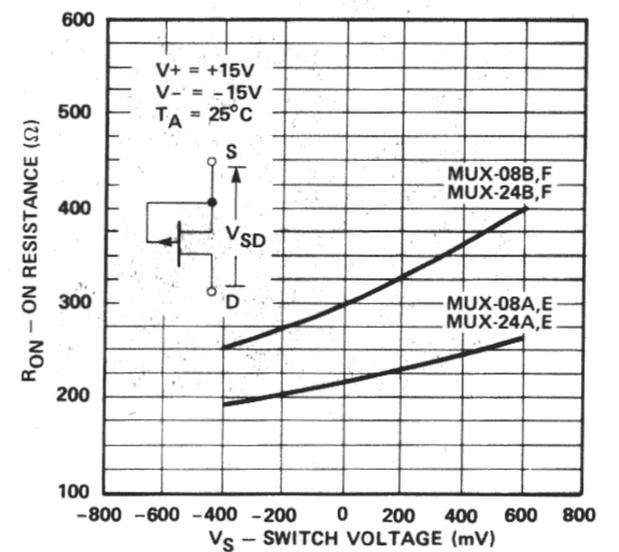
ENABLE DELAY TIMES vs TEMPERATURE



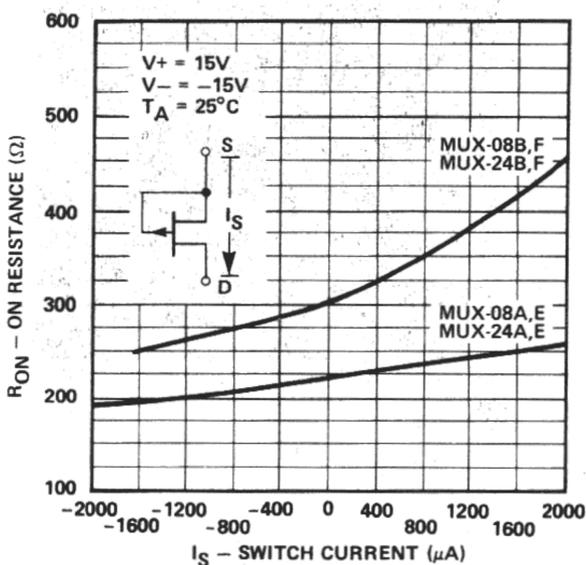
"ON" RESISTANCE (R_ON) vs ANALOG VOLTAGE (V_A)



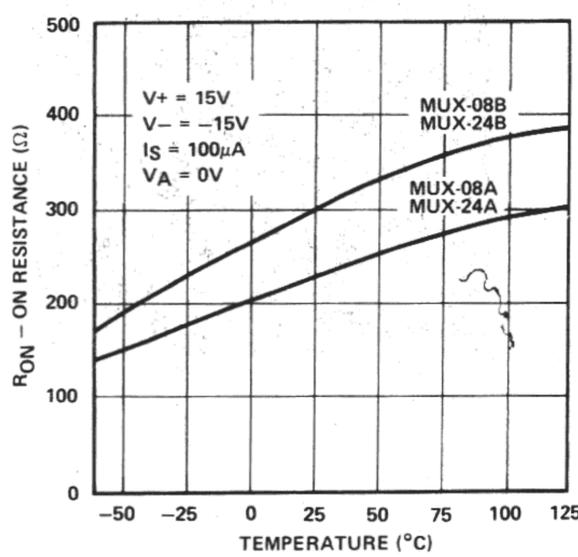
R_ON vs SWITCH VOLTAGE (V_SD)



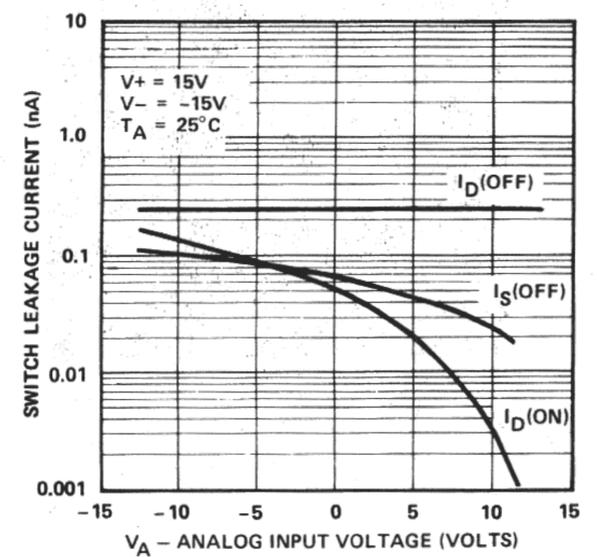
R_ON vs SWITCH CURRENT (I_S)



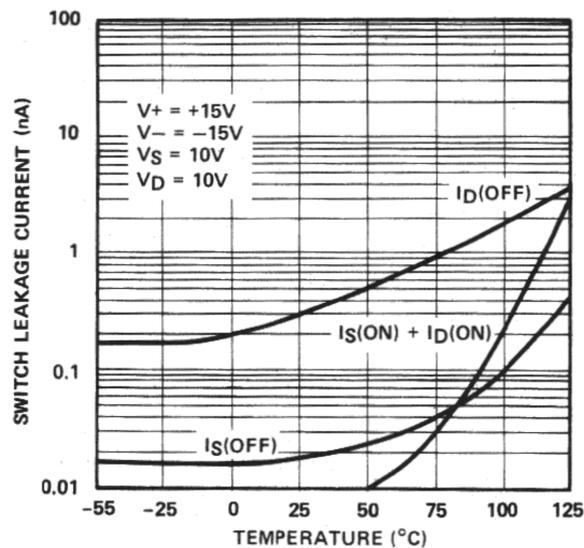
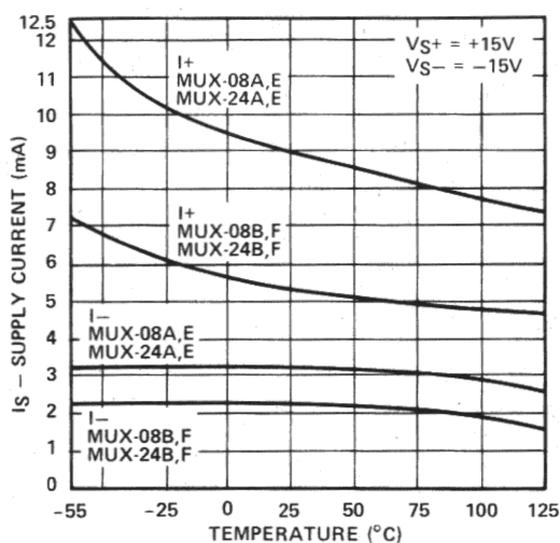
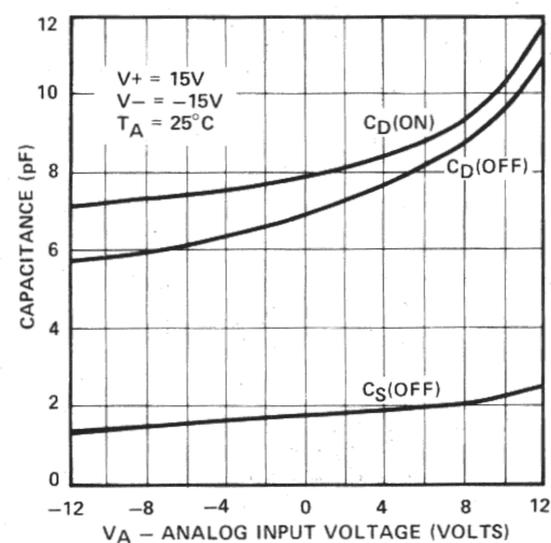
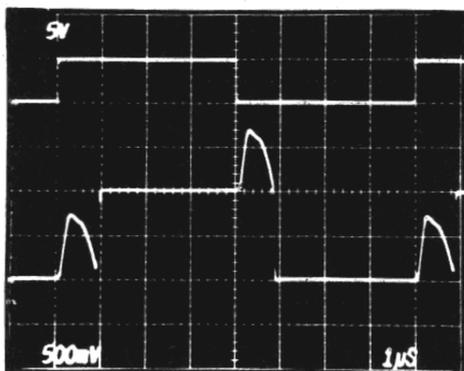
R_ON vs TEMPERATURE



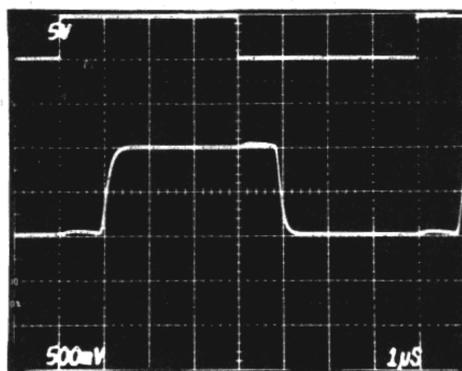
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



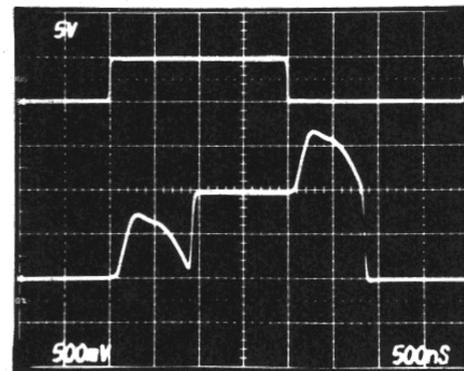
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

SWITCH LEAKAGE CURRENTS vs TEMPERATURE

SUPPLY CURRENTS vs TEMPERATURE

MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

MUX-24 SMALL-SIGNAL SWITCHING


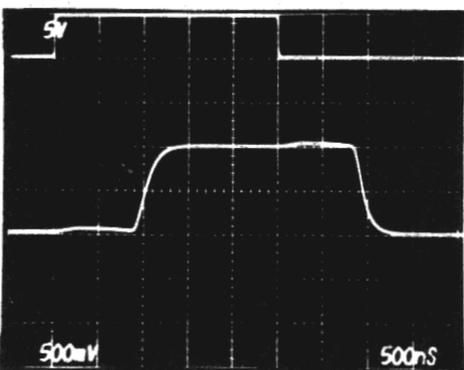
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING


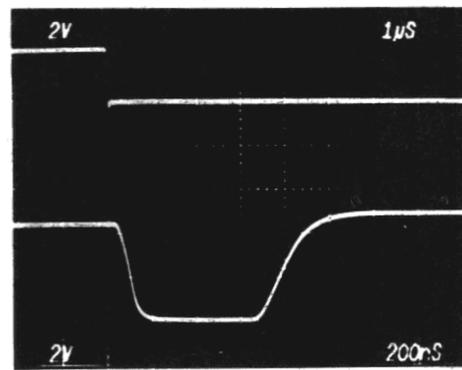
$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME


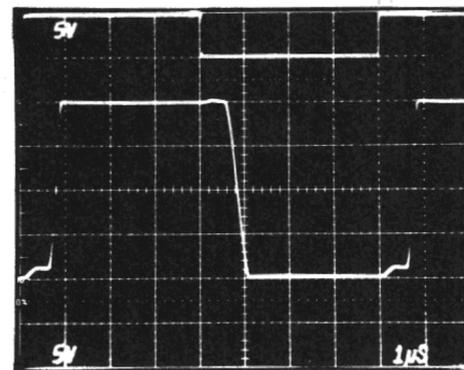
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME


$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING


$R_L = 1k\Omega$, $C_L = 10pF$, $V_1, 4 = 10V$
 VOLTAGE = 2V/DIV, TIME = 200ns/DIV

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MUX-24 LARGE-SIGNAL SWITCHING


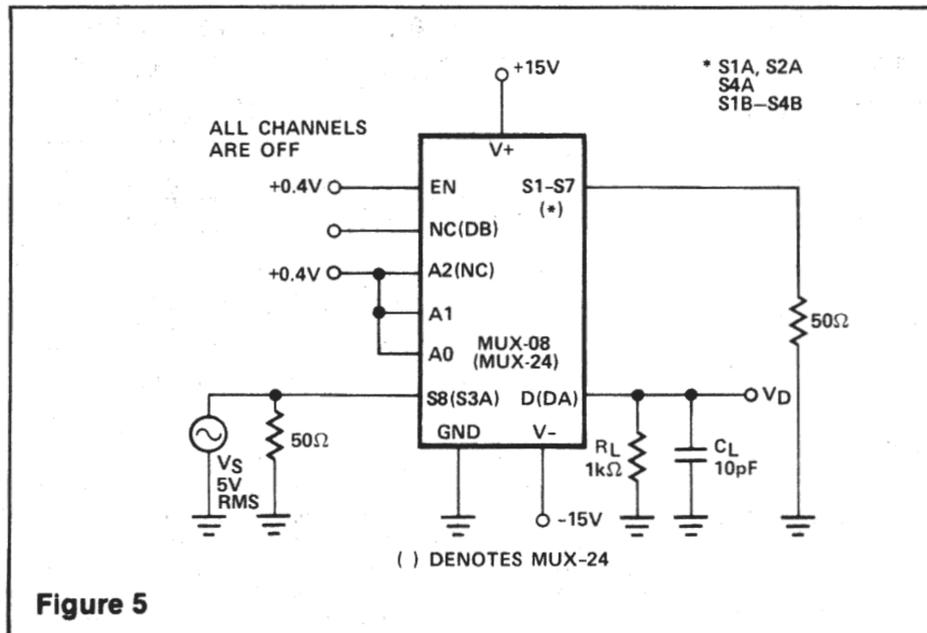
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_4 = +10V$
 VOLTAGE = 5V/DIV, TIME = 1µs/DIV

NOTE:

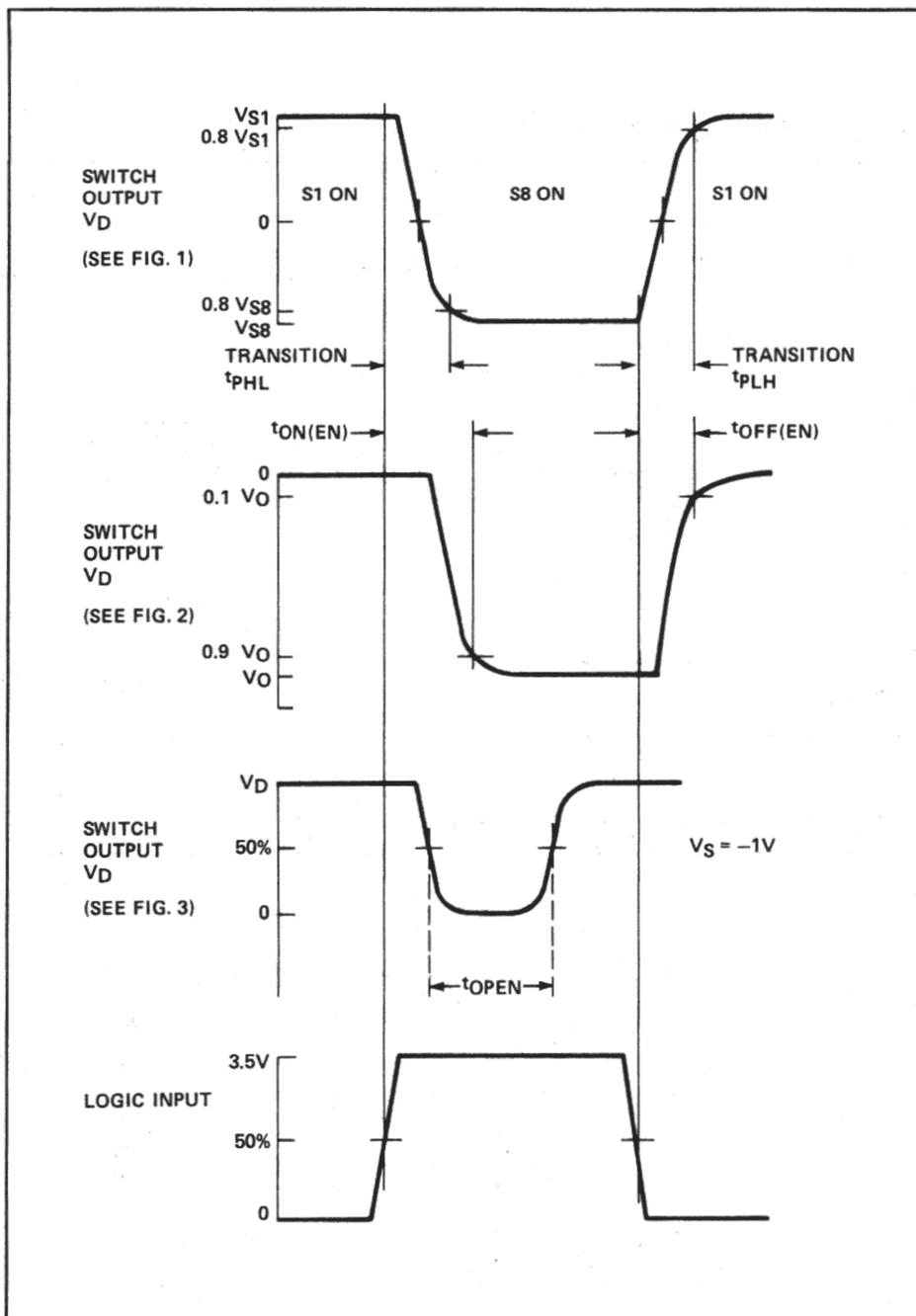
Top waveforms: Digital Input 5V/DIV
 Bottom waveforms: Multiplexer Output

A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT



SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p , and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu s$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu s$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

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CROSSTALK AND OFF-ISOLATION

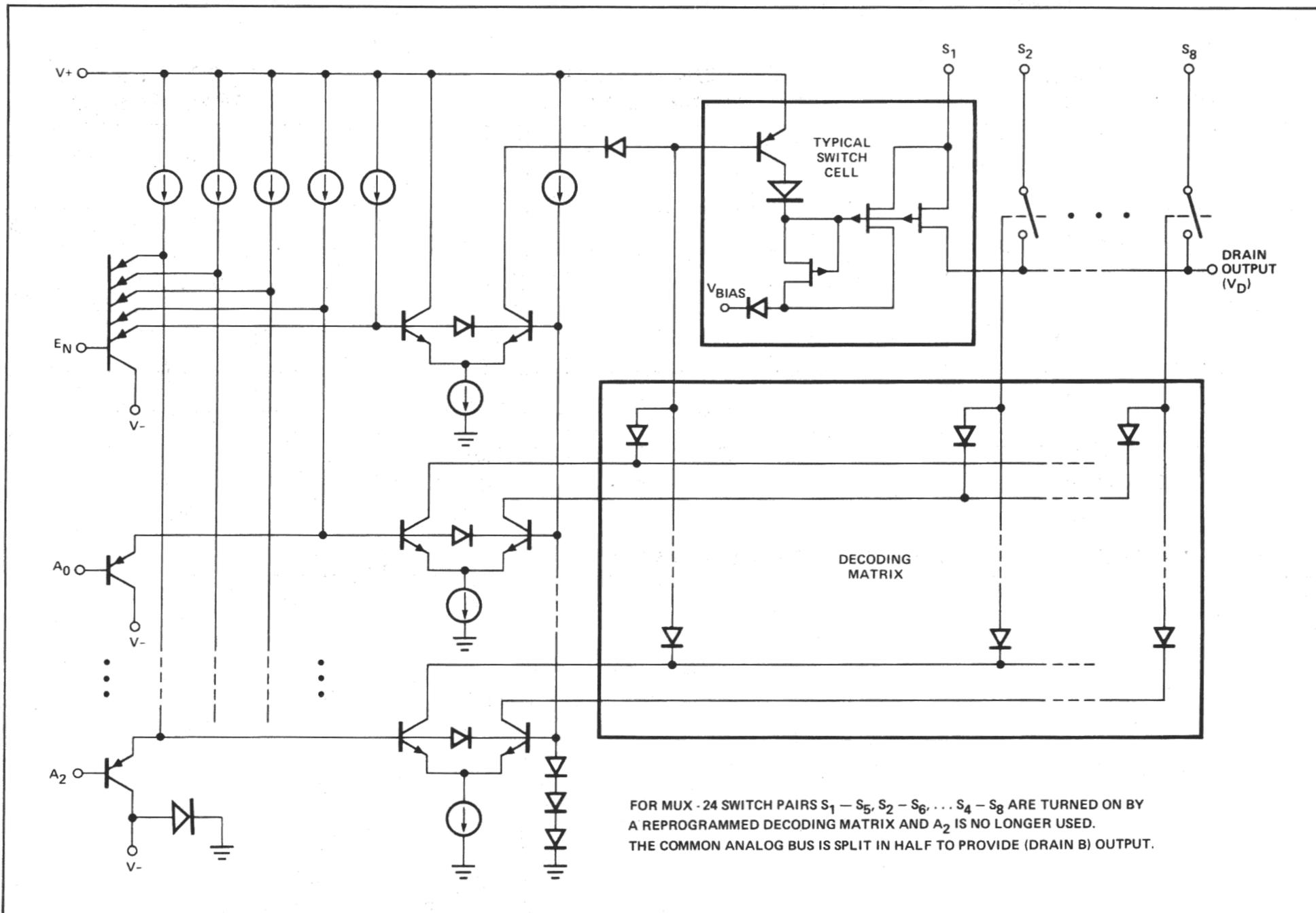
Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

SIMPLIFIED MUX-08 SCHEMATIC



The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V_- and ground prevents excessive current flow between V_+ and ground in the event that V_- becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

DIFFERENTIAL MULTIPLEXERS

One characteristic unique to differential multiplexers (MUX-24) is the ability to reject common-mode signals from becoming differential error signals. Common-mode rejection is a parameter which defines the amount of rejection in terms of dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at 400Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT

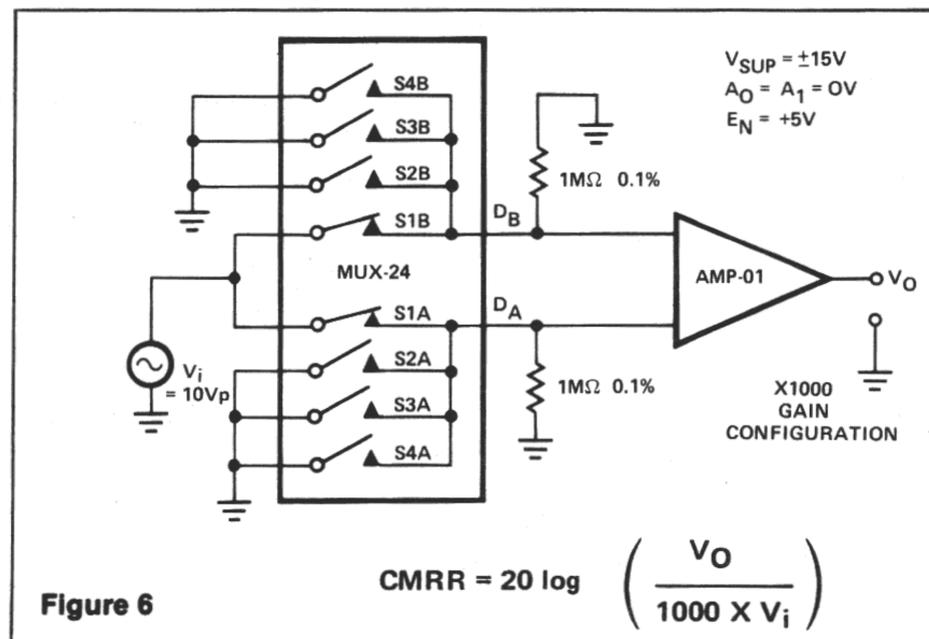
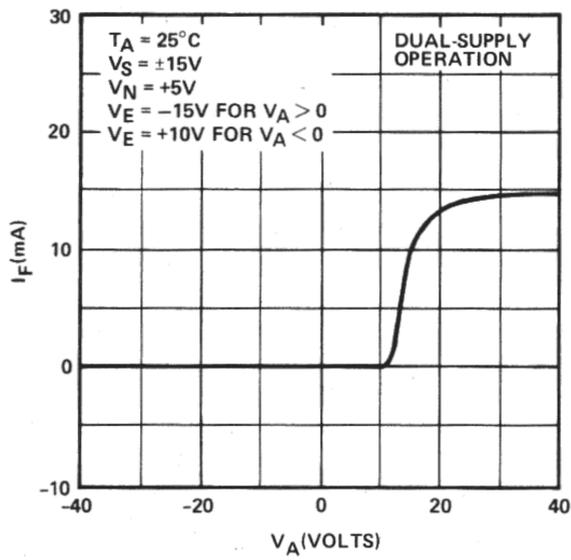


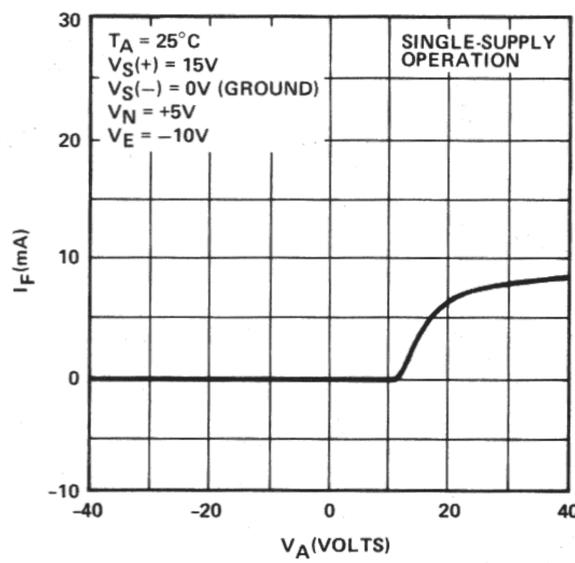
Figure 6

TYPICAL PERFORMANCE CHARACTERISTICS

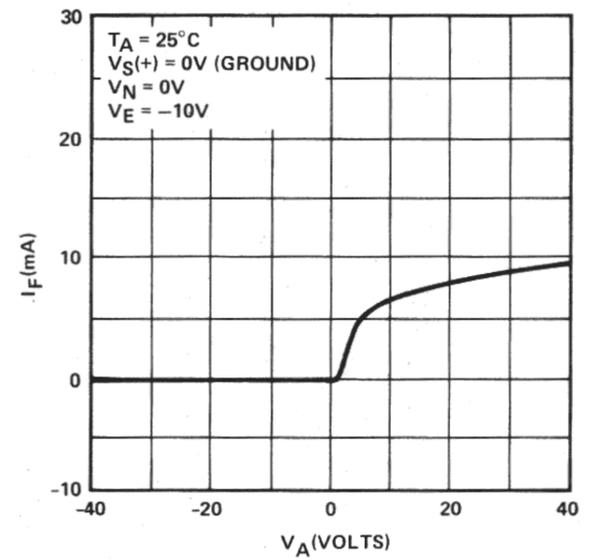
OVERVOLTAGE V-I CHARACTERISTIC



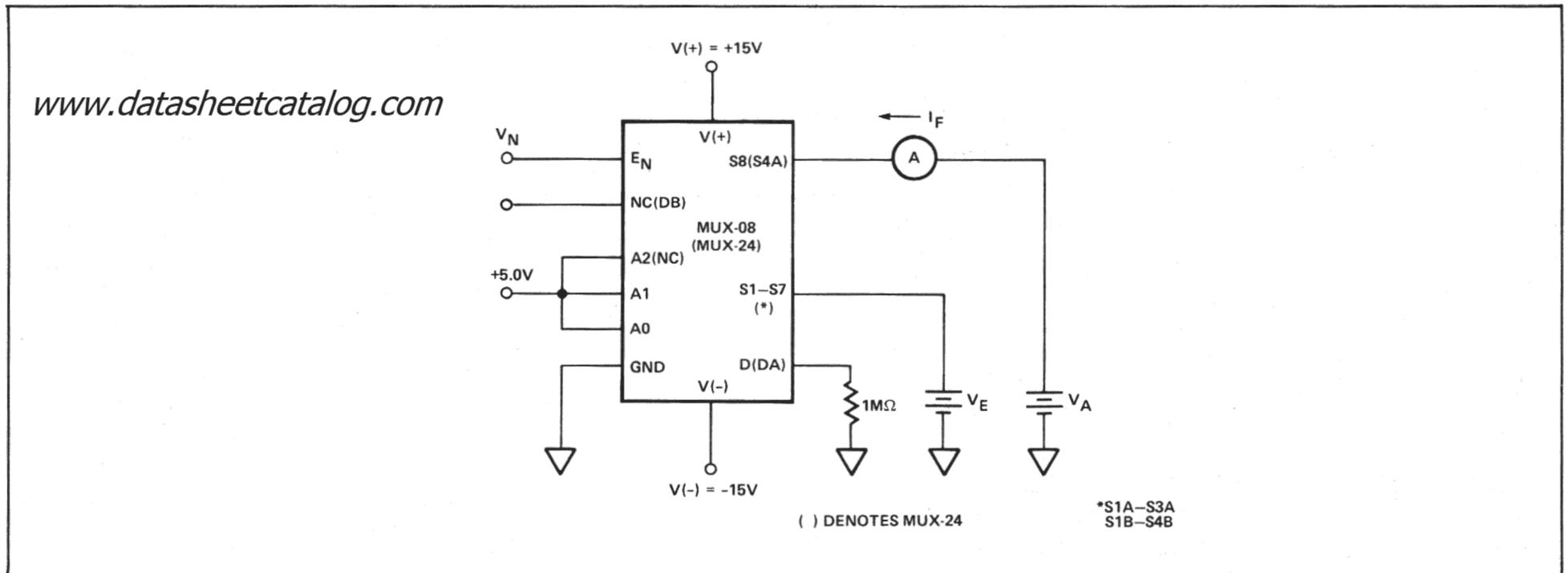
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



ANALOG SWITCHES MULTIPLEXERS

INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — the bipolar-JFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low "R_{ON}" resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent "R_{ON}" may typically be over 1000 ohms.

JFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low "R_{ON}" resistance. In addition, the special handling required with CMOS devices is not necessary with JFET switches.

In selecting analog multiplexers, attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by "R_{ON}" resistance and "C_{OUT}" capacitance specifications. A low "R_{ON}" insures minimum signal attenuation and maximum accuracy. The "C_{OUT}" capacitance forms on R-C time constant

with "R_{ON}" placing fundamental limits on signal acquisition time. Low "R_{ON}" and "C_{OUT}" insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

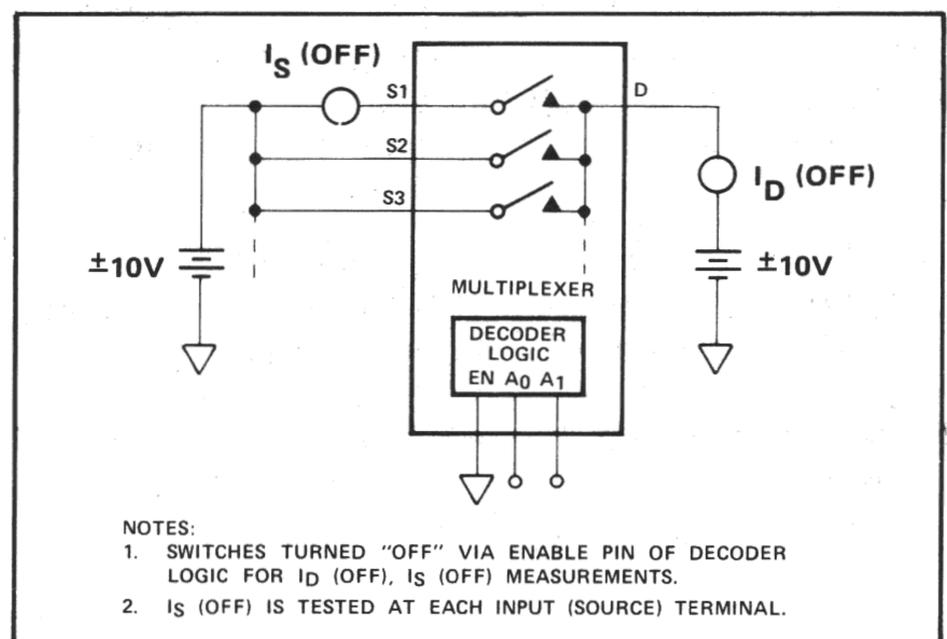
Two new additions to PMI's analog switch product offering are the SSM-2402 and SSM-2412. These dual channel devices provide *click-free* switching in audio applications.

DEFINITIONS

Analog Current Range (I_A, I_S) — The minimum range of currents the switch is capable of conducting in the ON state without degrading ON resistance. It is measured as the value of conduction current that does not cause more than a doubling of the R_{ON} value for the product grade.

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I_D(OFF), I_S(OFF) Test Condition Definitions





ANALOG SWITCHES MULTIPLEXERS

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Analog Input Leakage Current ($I_{S(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel source input to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output Leakage Current ($I_{D(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output-To-Input Capacitance ($C_{DS(OFF)}$) — The equivalent capacitance which shunts an open switch effectively between "S" and "D" output.

Analog Input Capacitance ($C_{S(ON)}$) — The capacitance between an analog "S" input and ground with the channel ON.

Analog Input Capacitance ($C_{S(OFF)}$) — The capacitance between an analog "S" input and ground with the channel OFF.

Analog Output Capacitance ($C_{D(OFF)}$) — The capacitance between the analog (DRAIN) output and ground with the channel OFF. High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON} .

Analog Output Capacitance ($C_{D(ON)}$) — The capacitance between the analog "D" output and ground with the channel ON.

Analog Voltage Range (V_A) — The range of analog-voltage amplitudes, with-respect-to-ground, over which the analog switch operates (ON/OFF) within the R_{ON} and leakage specifications — $I_{S(OFF)}$, $I_{D(OFF)}$ and $I_{D(ON)} + I_{S(ON)}$.

Break-Before-Make Delay (t_{OPEN}) — The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance ($C_{SS(OFF)}$, $C_{DD(OFF)}$) — The capacitance between the D(S) terminals of any two channels.

Charge Transfer (Q) — Charge transfer appears as a voltage step (pedestal) on the output capacitor after switch turn OFF. The undesirable charge AC couples directly from the logic-control driver to the switch contact.

Crosstalk (CT) — The proportionate amount of cross-coupling from an analog input channel to another output channel, expressed in dB.

Digital Input Capacitance (C_{DIG}) — The capacitance between a digital input and ground.

Insertion Loss — Insertion loss measures the amount of signal power absorbed by the switch ON resistance at a given measurement frequency. Insertion loss is defined in decibels as a ratio of the output-voltage amplitude (V_D) versus the input-voltage amplitude (V_S) with a specified load impedance.

$$\text{Insertion Loss (dB)} = 20 \log \frac{|V_D|}{|V_S|}$$

At low frequencies this equation simplifies to:

$$\text{Insertion Loss (dB)} = 20 \log \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "0" Input Current (I_{INL}) — The current flowing into a digital input when a specified low-level voltage is applied to that input.

Logic "0" Input Voltage Level (V_{INL}) — The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

Logic "1" Input Voltage Level (V_{INH}) — The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

Negative Voltage Supply (V^-) — The most negative voltage supply with respect to ground.

Positive Voltage Supply (V^+) — The most positive voltage supply with respect to ground.

ANALOG SWITCHES MULTIPLEXERS

OFF Isolation ($ISO_{(OFF)}$) — The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

ON Resistance (R_{ON}) — The series ON - channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match (R_{ON} Match) — The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

$$R_{ON} \text{ Match} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

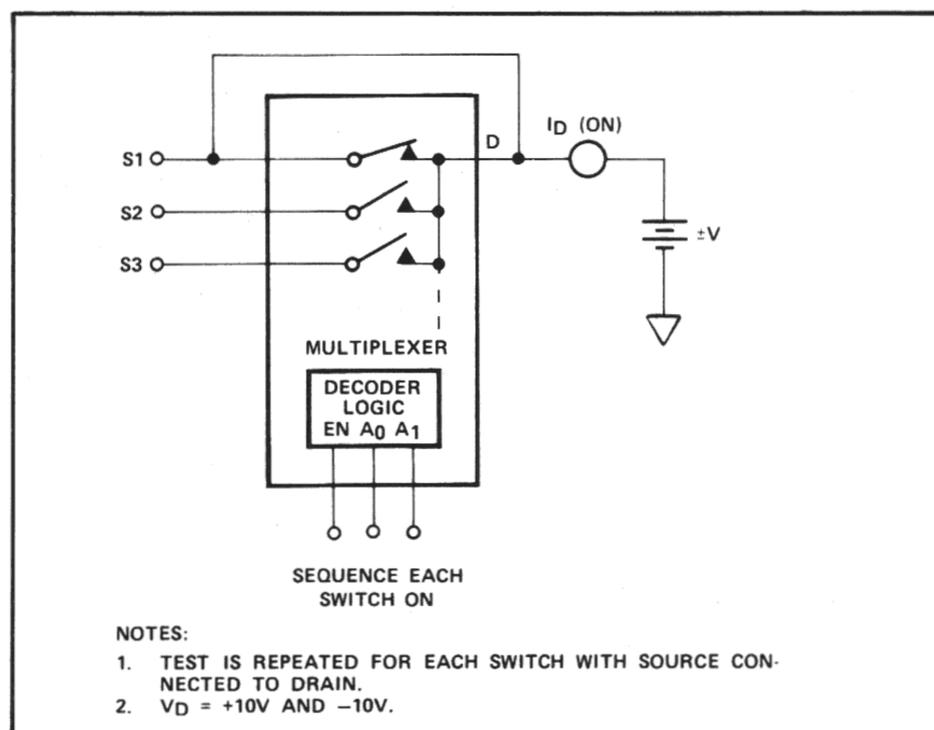
N = # of channels in package (i.e., for MUX-08

N = 8, for MUX-16 N = 16, etc.)

R_i = Each channel's ON resistance

$$R_{AVG} = \frac{1}{N} \sum_{i=1}^N R_i$$

$I_{(ON)}$ Test Condition Definitions



ON Resistance Variation (ΔR_{ON}) — The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON} (\%) =$$

$$\frac{R_{ON} @ V_A = -10V - R_{ON} @ V_A = +10V}{R_{ON} @ V_A = 0V} \times 100\%$$

ON Channel Analog Leakage Current ($I_{D(ON)} + I_{S(ON)}$) Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

Output Enable Delay Time OFF ($t_{OFF(EN)}$) — Multiplexers — The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

Output Enable Delay Time ON ($t_{ON(EN)}$) — Multiplexers — The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

Output ON Switching Time (t_{ON}) — The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Output OFF Switching Time (t_{OFF}) — The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output Settling Time (t_s) — The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within specified error band.



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Power Supply Rejection (PSRR) — The ratio of the change in switch contact voltage (V_D) to the change in voltage supply ($V+$ or $V-$) that causes it.

$$+PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V+} \right)$$

$$-PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V-} \right)$$

Switching Time (t_{TRAN}) — Multiplexers — The time required to switch and slew from one

analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 80% of the final value.

Total Harmonic Distortion (THD) — The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).

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ANALOG SWITCHES/MULTIPLEXERS SELECTION GUIDE

One Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels		Supply Current (mA)	
		t_{ON}	t_{OFF}		V_{INL}	V_{INH}	I+	I-
SW01	100	0.4	0.3	0	0.8	2.0	8.0	4.5
SW02	100	0.4	0.3	1	0.8	2.0	8.0	4.5

2-Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels		Supply Current (mA)	
		t_{ON}	t_{OFF}		V_{INL}	V_{INH}	I+	I-
SSM2402	85	10000	4000	1	0.8	2.0	7.5	6.0
SSM2412	85	3500	1500	1	0.8	2.0	7.5	6.0

4-Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels		Supply Current (mA)	
		t_{ON}	t_{OFF}		V_{INL}	V_{INH}	I+	I-
SW06	80	0.5	0.4	Note	0.8	2.0	6.0	5.0
SW201	80	0.5	0.4	0	0.8	2.0	9.0	5.0
SW202	80	0.5	0.4	1	0.8	2.0	9.0	5.0
SW7510	75	0.45	0.3	Note	0.8	2.0	9.0	5.0
SW7511	75	0.45	0.3	Note	0.8	2.0	9.0	5.0

NOTE: See individual data sheet for more details.



ANALOG SWITCHES MULTIPLEXERS

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8-Channel MUX

Product	R _{ON} Max (Ω)	Transition Time (μs)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX08	300	2.1	0.7	2.0	12.0	3.8
MUX88	400	2.1	0.8	2.0	15.0	5.0

Dual 4-Channel MUX

Product	R _{ON} Max (Ω)	Transition Time (μs)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX24	300	2.1	0.7	2.0	12.0	3.8

16-Channel MUX

Product	R _{ON} Max (Ω)	Transition Time (μs)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX16	380	2.0	0.7	2.0	19.0	7.0

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Dual 8-Channel MUX

Product	R _{ON} Max (Ω)	Transition Time (μs)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX28	380	2.0	0.7	2.0	19.0	7.0