

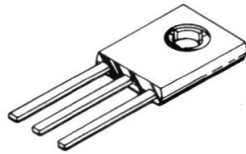
**2N5190 (SILICON)**  
thru  
**2N5192**



Silicon NPN power transistors for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195.

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**MAXIMUM RATINGS**



**CASE 77(1)**

Rating	Symbol	2N5190	2N5191	2N5192	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	40	60	80	Vdc
Collector Current	$I_C$	4.0			A dc
Base Current	$I_B$	1.0			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 320			Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage* ( $I_C = 0.1 \text{ A dc}, I_B = 0$ )	2N5190 2N5191 2N5192	$BV_{CEO(sus)}^*$	40 60 80	- - -	Vdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 60 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 80 \text{ Vdc}, I_B = 0$ )	2N5190 2N5191 2N5192	$I_{CEO}$	- - -	1.0 1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 40 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ )	2N5190 2N5191 2N5192 2N5190 2N5191 2N5192	$I_{CEX}$	- - - - - -	0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ( $V_{CB} = 40 \text{ Vdc}, I_E = 0$ ) ( $V_{CB} = 60 \text{ Vdc}, I_E = 0$ ) ( $V_{CB} = 80 \text{ Vdc}, I_E = 0$ )	2N5190 2N5191 2N5192	$I_{CBO}$	- - -	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}, I_C = 0$ )		$I_{EBO}$	-	1.0	mAdc

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

**2N5190 thru 2N5192 (continued)**

(continued)

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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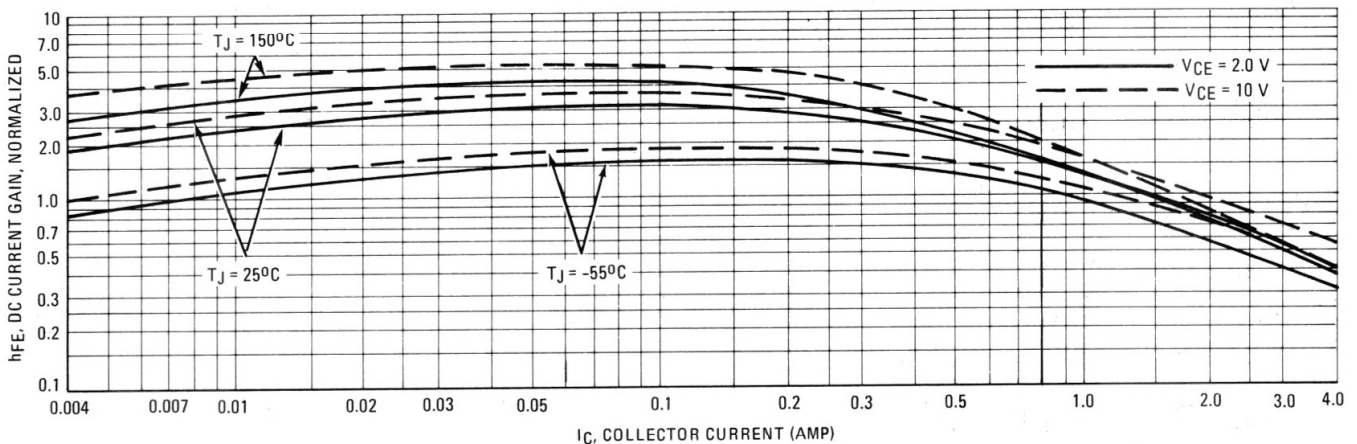
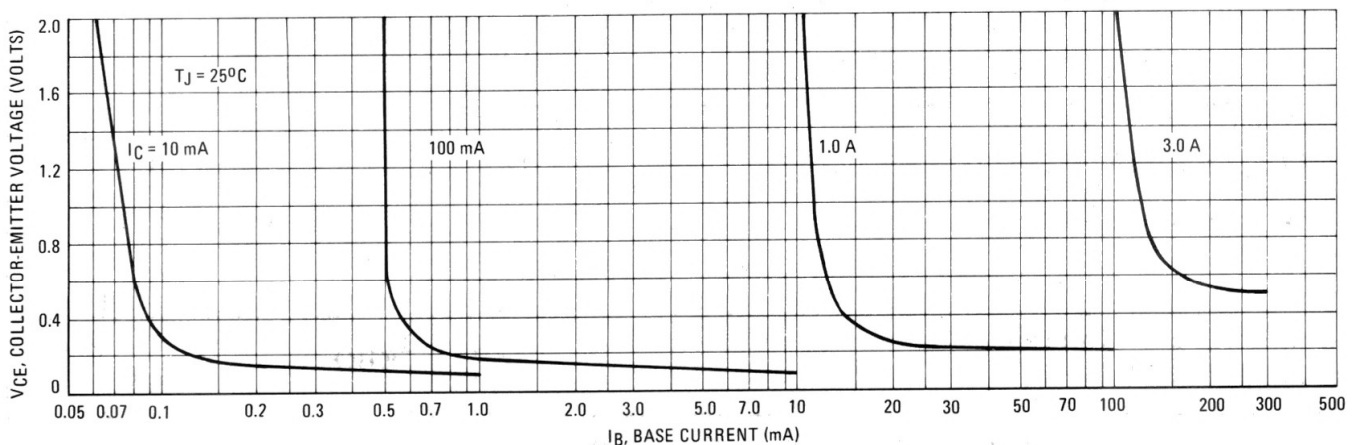
**ON CHARACTERISTICS**

DC Current Gain* ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5190, 2N5191, 2N5192 2N5190, 2N5191, 2N5192	$h_{FE}^*$	25 20 10 7.0	100 80 - -	-
Collector-Emitter Saturation Voltage* ( $I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$ ) ( $I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$ )		$V_{CE(sat)}^*$	-	0.6 1.4	Vdc
Base-Emitter On Voltage* ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )		$V_{BE(on)}^*$	-	1.2	Vdc

**DYNAMIC CHARACTERISTICS**

Current-Gain-Bandwidth Product ( $I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$f_T$	2.0	-	MHz
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 \*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

**FIGURE 1 – NORMALIZED DC CURRENT GAIN**

**FIGURE 2 – COLLECTOR SATURATION REGION**


# 2N5190 thru 2N5192 (continued)

FIGURE 3 – "ON" VOLTAGES

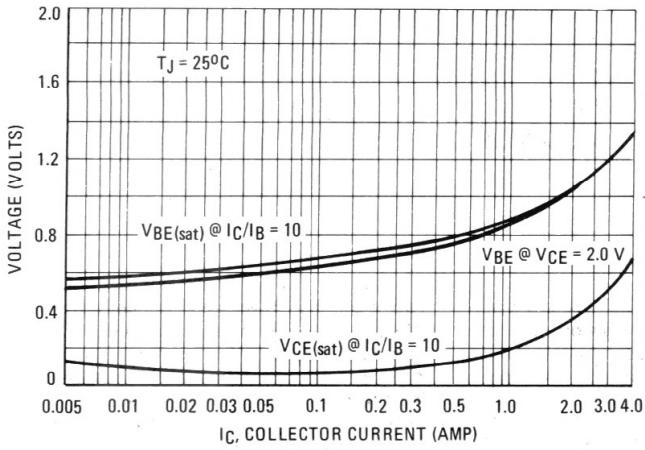
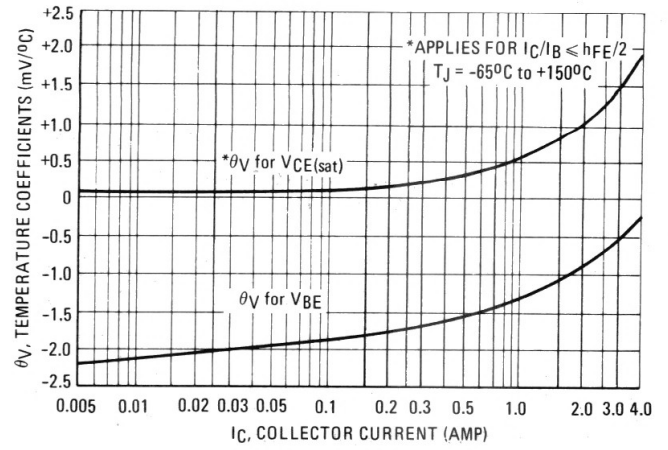


FIGURE 4 – TEMPERATURE COEFFICIENTS



## TYPICAL "OFF" REGION CHARACTERISTICS

FIGURE 5 – COLLECTOR CUT-OFF REGION

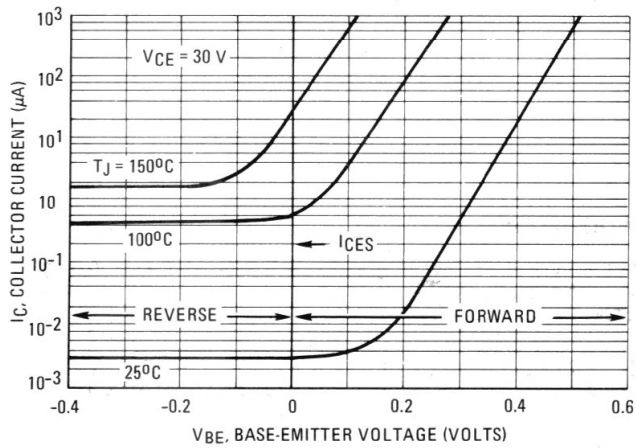


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

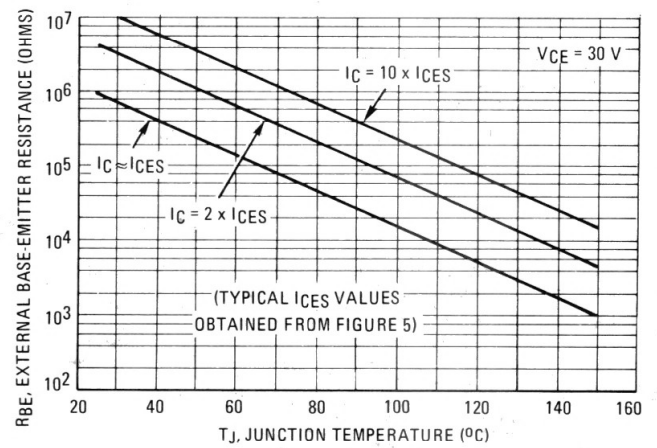


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

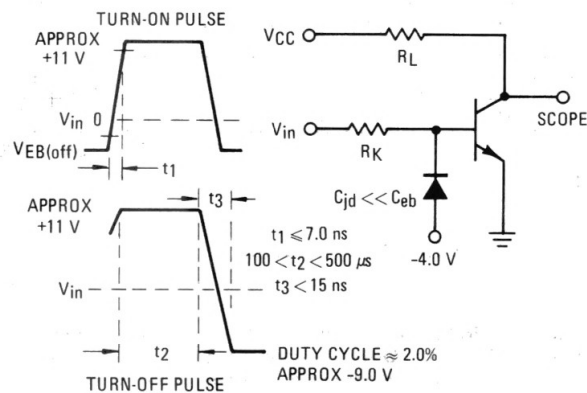


FIGURE 8 – CAPACITANCE

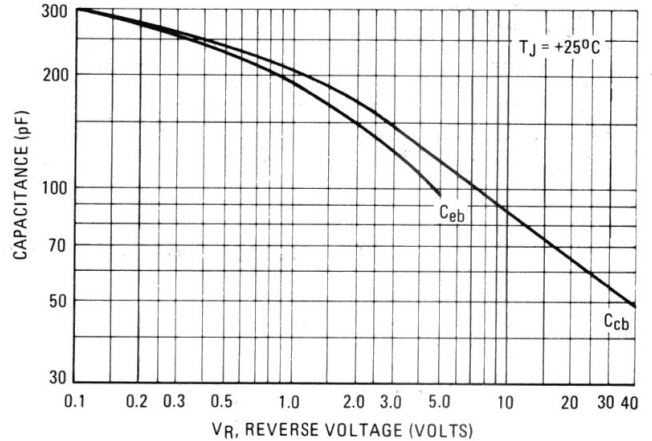


FIGURE 9 – TURN-ON TIME

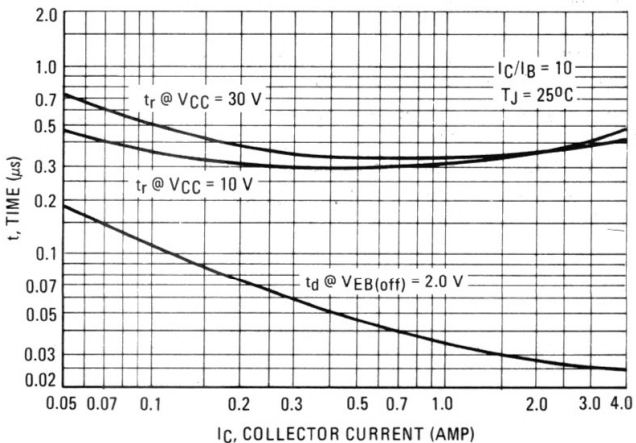
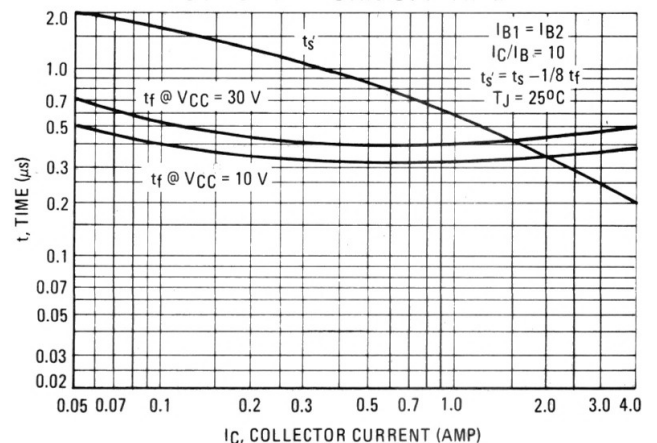
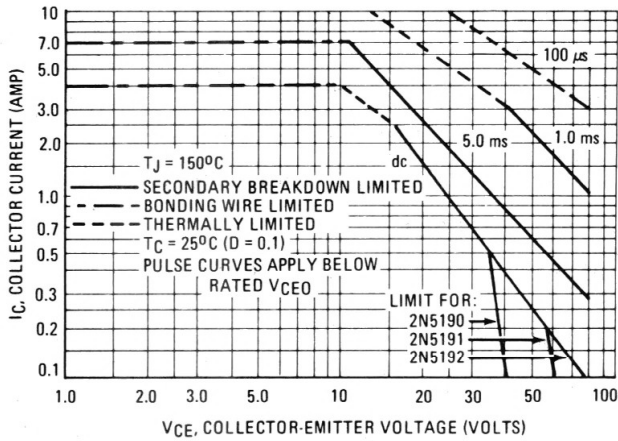


FIGURE 10 – TURN-OFF TIME



**RATING AND THERMAL DATA**

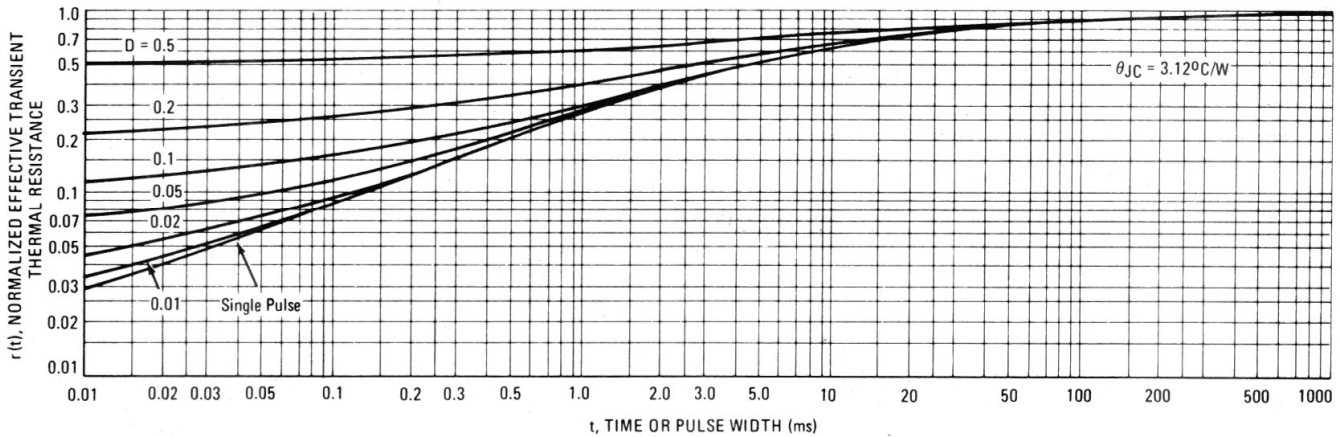
**FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA**



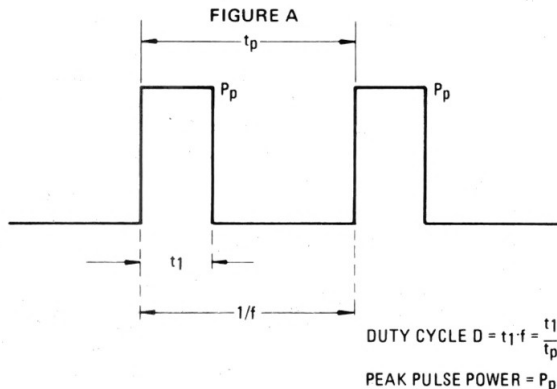
There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

**FIGURE 12 – THERMAL RESPONSE**



**DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA**



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5190 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$