PLESSEY
Semiconductors

SP8620A & B

400MHz ÷ 5

The SP8620 is an asynchronous emitter coupled logic counter which provides ECL compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

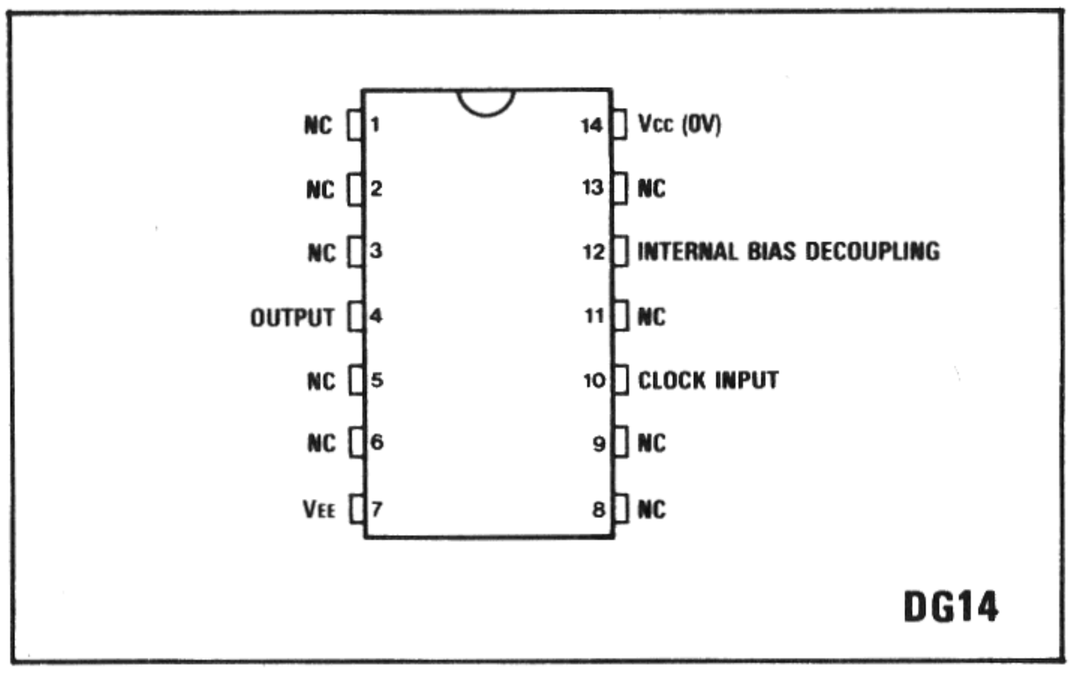

Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 285mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +150°C
- Max. Clock I/P Voltage: 2.5V p-p

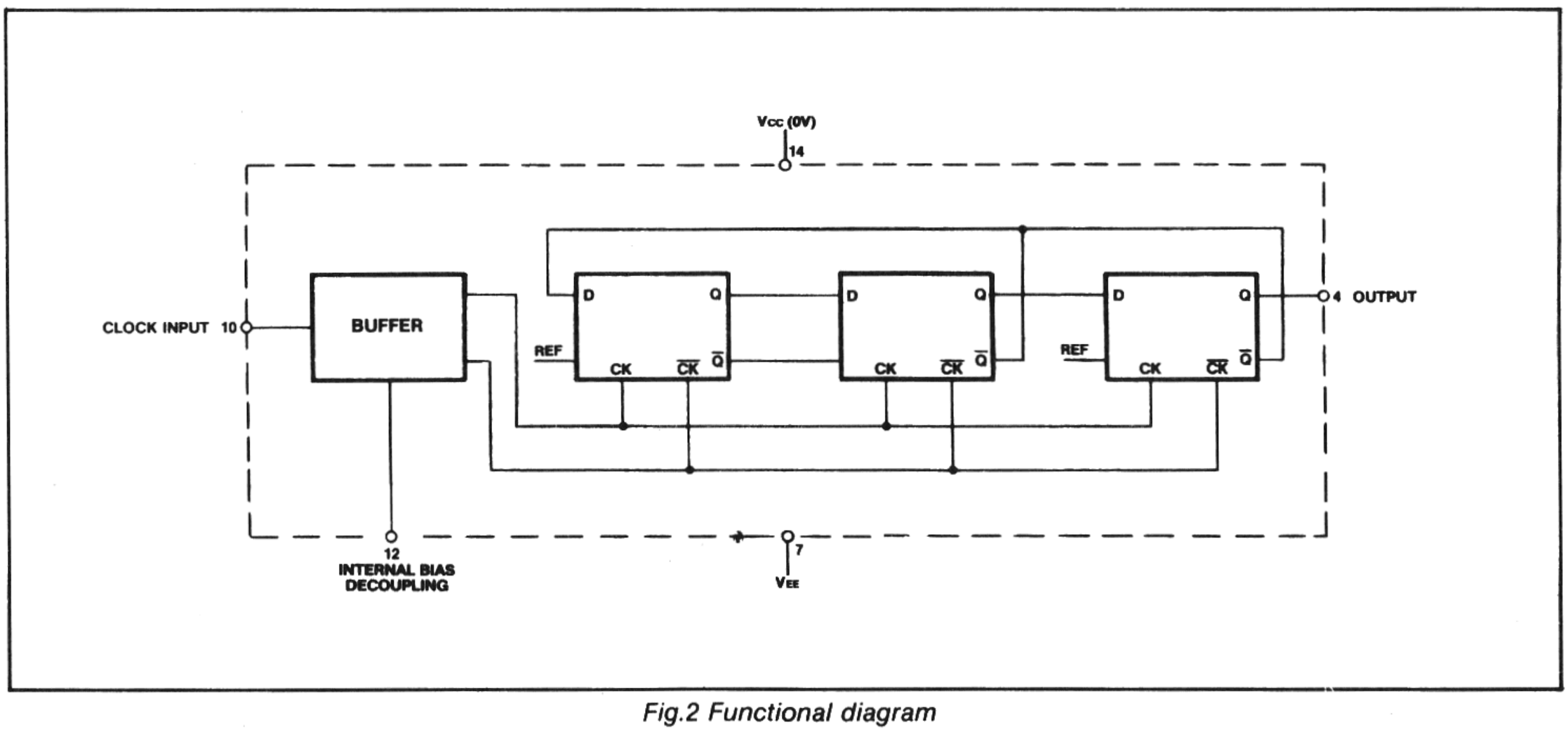

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Temperature
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	400		MHz	Input = 400-800mV p-p	As specified
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	As specified
Power supply current	I_{EE}		55	mA	V_{EE} = -5.2V	As specified
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V	25°C
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V	25°C
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	As specified

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C.
3. The test configuration for dynamic testing is shown in Fig. 5.

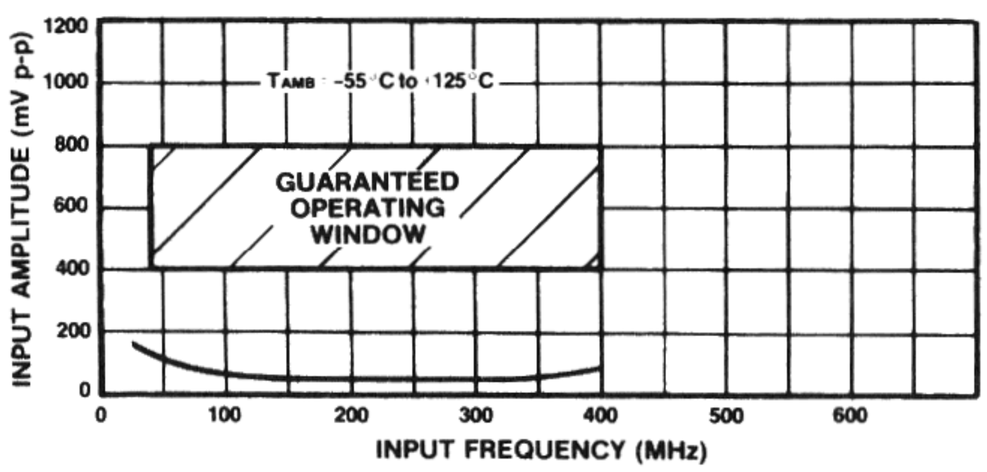

Fig.3 Typical input characteristic of SP8620A

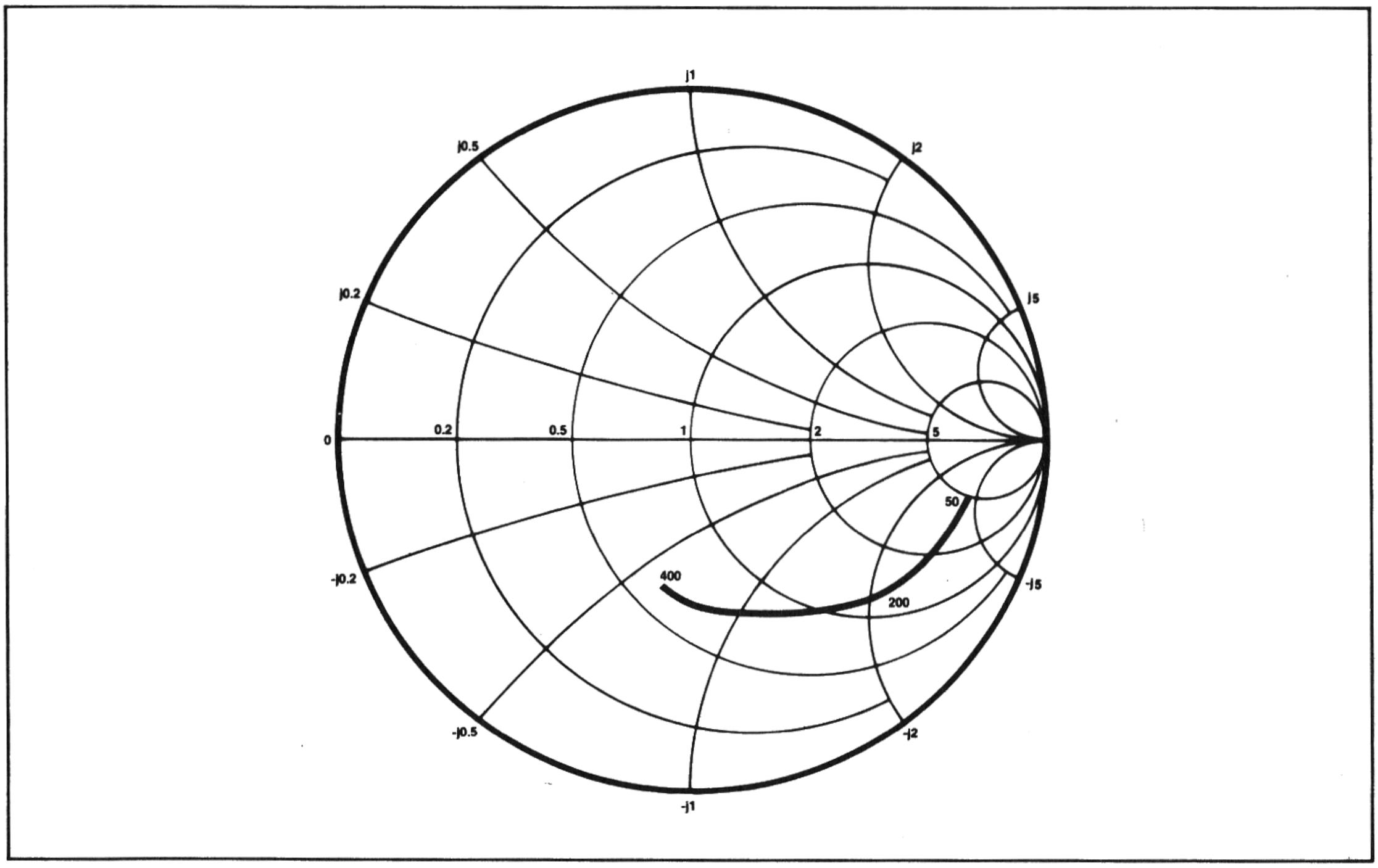

Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the clock input to V_{EE} (ie Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 3k at the output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

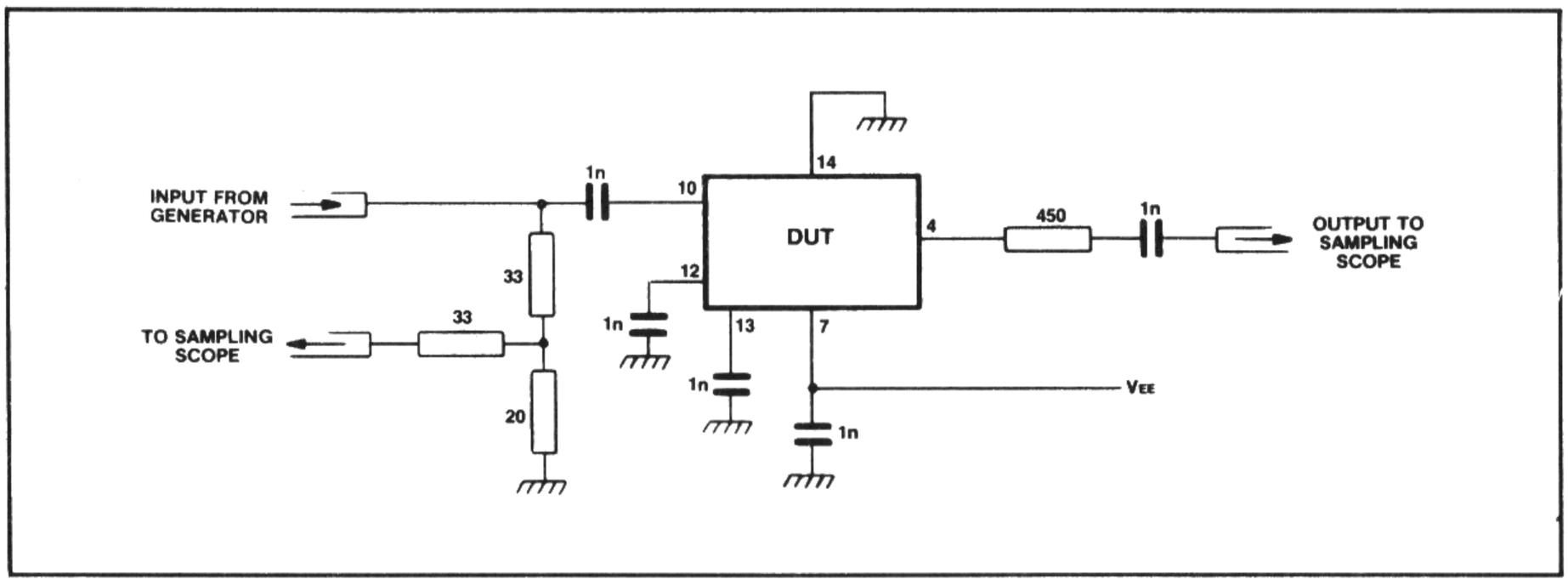

Fig.5 Test circuit

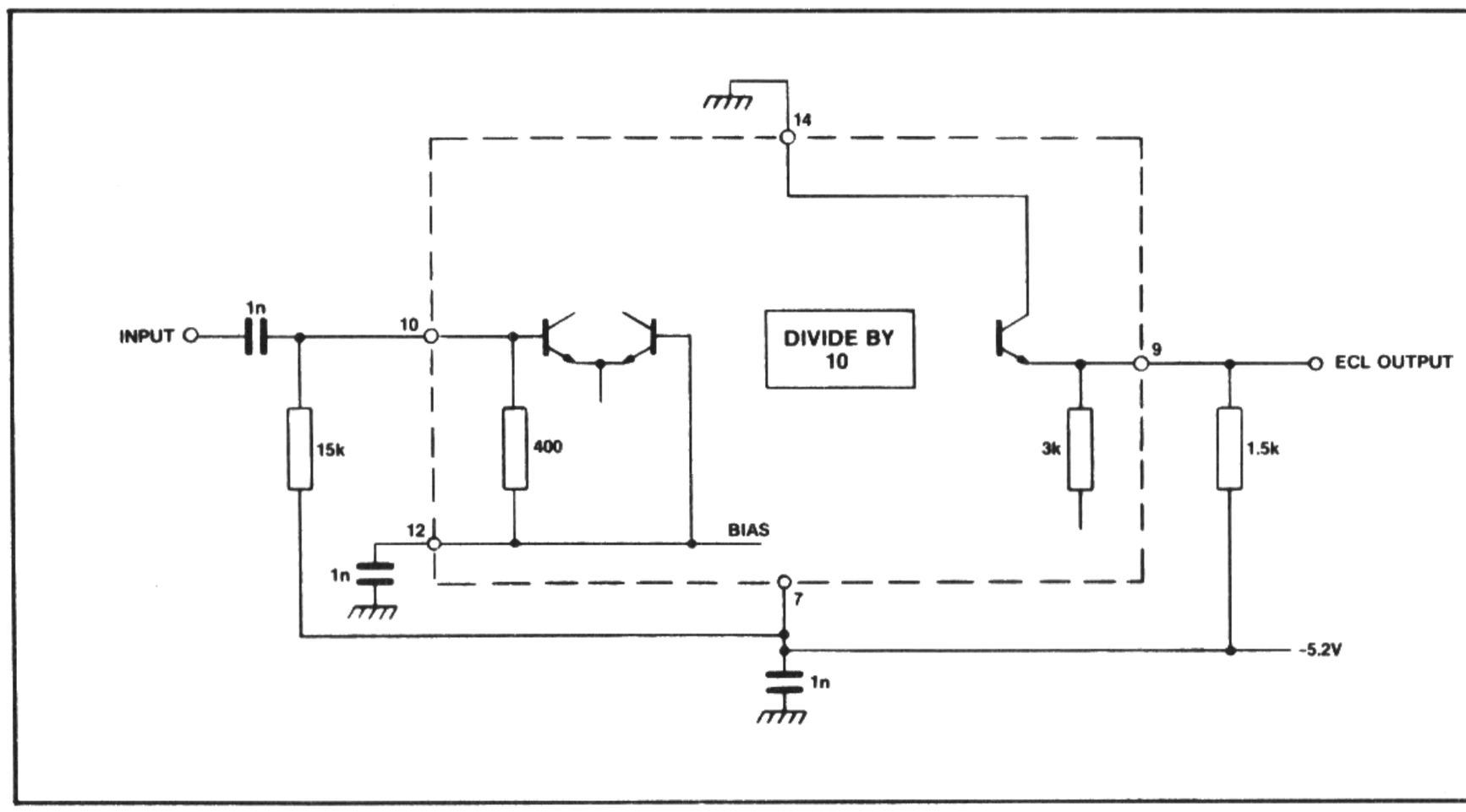

Fig.6 Typical application showing interfacing